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Ternary logic to binary bit conversion using multiple input floating gate MOSFETS in 0.5 micron n-well CMOS technology

Sowmya Subramanian
Louisiana State University and Agricultural and Mechanical College

TERNARY LOGIC TO BINARY BIT CONVERSION USING MULTIPLE INPUT FLOATING GATE MOSFETS IN 0.5 MICRON N-WELL CMOS TECHNOLOGY

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To
My Family

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ABSTRACT

In the present work, a CMOS ternary to binary bit conversion technique has been proposed using multiple input floating gate MOSFETs. The proposed circuit has been implemented in 0.5 μm n-well CMOS technology. The ternary input signals of {-1, 0, +1} are represented as -3 V, 0 V and +3 V, respectively. The ternary input is given as a combination of any two of the three voltage levels and the 4-bit binary output is generated in which the left most bit is sign bit (SB) followed by most significant bit (MSB), second significant bit (SSB) and the least significant bit (LSB).

The potential on the floating gate can be modified by either capacitive coupling with other conductors or by changing the stored charge on the floating gate. After each computation for a certain combination of inputs the floating gate carries a specific charge which has to be removed, or compensated for in order, to maintain integrity of the next computation. The four methods used commonly for modifying stored charge on the floating gate are UV radiation, tunneling, channel hot-electron injection and hopping through or trapping/de-trapping of charges. A simple method has been presented where the residual charge on the floating gate is by-passed and set to a certain biased initial value. Based on this initial value for the floating node voltage, the ratios of the values of the input capacitors which are capacitively coupled to the floating gate have been designed. The design was simulated in PSPICE and the output voltage at each stage of the converter was used to back calculate and model the ratios for the input capacitors as well as determine the biasing voltage on the floating gate.

Chapter 1. Introduction and Literature Search

1.1 Introduction

Multiple-valued logic (MVL) has more than two discrete logical states and the ability to carry additional information in comparison to binary logic [1 - 4]. Though MVL has yet to make a place among binary logic design engineers [23] due to difficulty in design, ternary and quaternary valued logic have started gaining significance [5 - 8] due to ease in design. In this work, an attempt has been made to simplify the ternary-to-binary bit conversion design in multiple-input floating gate MOSFETS in CMOS.

Ternary values for a system can be {0, 1, 2} (simple unsigned), or can be redefined as {-1, 0, +1} (balanced signed). The ternary input signals of {-1, 0, +1} can be represented by negative voltage, zero voltage, and positive voltage respectively, as shown in Figure 1.1 [8]. In ternary logic for positive numbers the most significant non-zero digit is always +1; if negative numbers are considered, then by changing all +1's to -1's and vice versa, leaving all zeroes unchanged, gives the negative of the corresponding number. Hence it follows that addition and subtraction may be performed with the same hardware in the balanced ternary system by sign changes of the addend or subtrahend, respectively.

1.2 Literature Search

Floating gate MOS circuits have been developed in CMOS processes primarily by using two levels of polysilicon [9]. Minch and Hasler [10] have presented a design where only one layer of polysilicon is used to build high performance floating gate memories and circuits in digital CMOS processes.

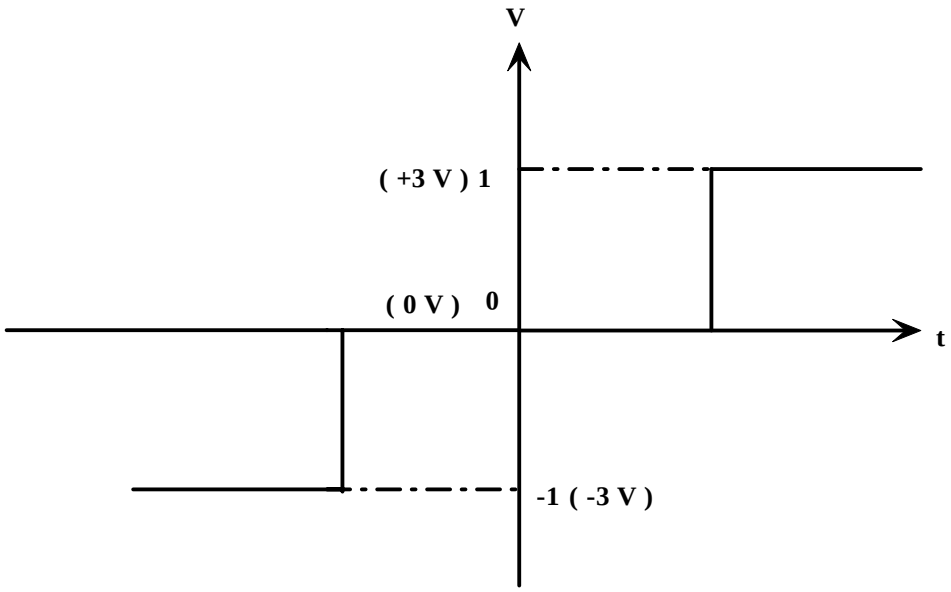

Figure 1.1. Ternary Input Logic Levels.

Mondragon-Torres *et al*. [11] have proposed well driven floating gate transistors, where the floating gate in MOS device is put on top of an n-well. The corresponding capacitive equivalent model is shown in Figure 1.2. The n-well provides the noise isolation for the floating gate MOSFET from the substrate and can also be used as an additional input for the control of threshold voltage or signal modulation. The potential on the floating gate can be modified by either capacitive coupling with other conductors or by changing the stored charge on the floating gate. The voltage on the floating gate can be expressed as [11]

$$V_{FG} = \sum_{i=1}^{N} \alpha_i V_i + \alpha_W V_W + V_{EQ} \tag{1.1}$$

where $\alpha_i = C_i / C_T$ is the i^{th} coupling coefficient. C_i represents the capacitance from the i^{th} controlling input V_i to the floating gate, N is the number of capacitors and C_T is the total floating gate capacitance at the floating gate. $\alpha_W = C_W / C_T$ is the coupling coefficient from the well input, V_w, to the floating gate. V_{EQ} is the equivalent voltage due to both the charges stored on the floating gate as well as the dc voltages at the source and drain that are capacitively coupled to the floating gate.

Kucic *et al.* [12] have discussed the reliability of floating gates in analog systems. These are following several methods which may modify the charge stored on the floating gate.

UV Radiation: UV exposure is performed through a glass cover in the package and can alter the charge on the floating gate.

Tunneling: Fowler Nordheim tunneling through thin oxides can modify the charge stored on a floating gate.

Channel hot-electron injection: In this process the charge on the floating gate is modified when the electron is accelerated due to high electric field at the drain.

Hopping through or Trapping/Detrapping: Defects in the oxide create states which can be occupied by electrons.

Ning *et al.* [13] presented a floating gate ac nulling (FGAN) technique to reduce residual charges on the floating gate as shown in Figure 1.3. Vin1 and Vin2 denote two DC terminals and s1 and s2 are switches used to generate AC signals which are controlled by a clock. M1 and R form a buffer which is used to measure the voltage on the floating gate and M2 is a MOSFET for setting the pre-charge on the floating gate. The circuit transforms the ratio of capacitors C1 and C2 to a ratio of voltages. If C1 and C2 are perfectly matched then it results in a null AC component of voltage on the floating gate, provided Vin1 and Vin2 are at the same voltage level. If the capacitors are mismatched then there is an ac component on the floating gate which can be compensated only by varying Vin2. The ratio mismatch of the capacitors C1 and C2 can be represented as a ratio of voltages Vin1 and Vin2 given by the equation,

$$\frac{C_2 - C_1}{C_2} = \frac{V_{in1} - V_{in2}}{V_{in1}}. \tag{1.2}$$

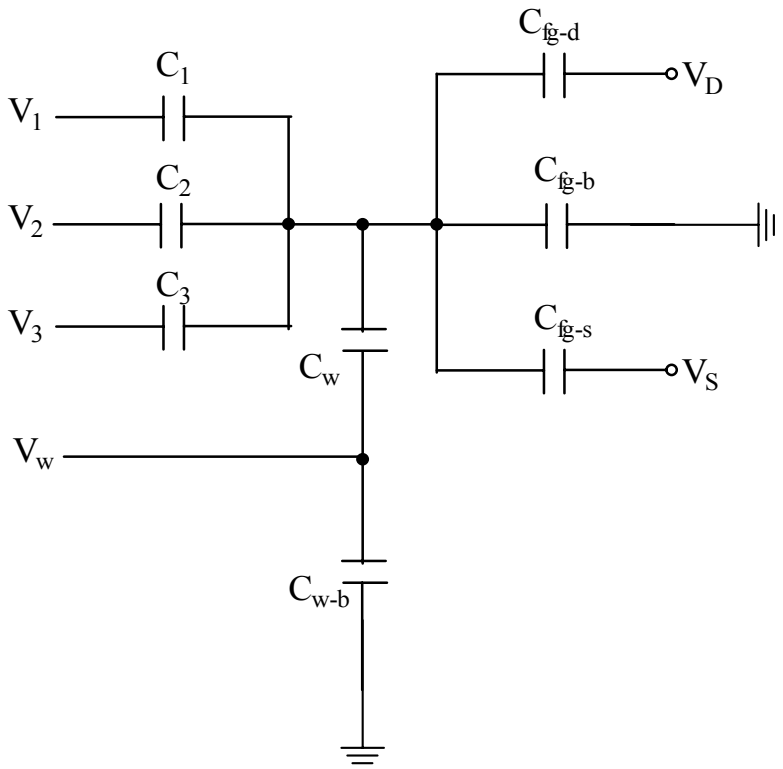

Figure 1.2. Equivalent Capacitive Model of a Well Driven Floating Gate Transistor.

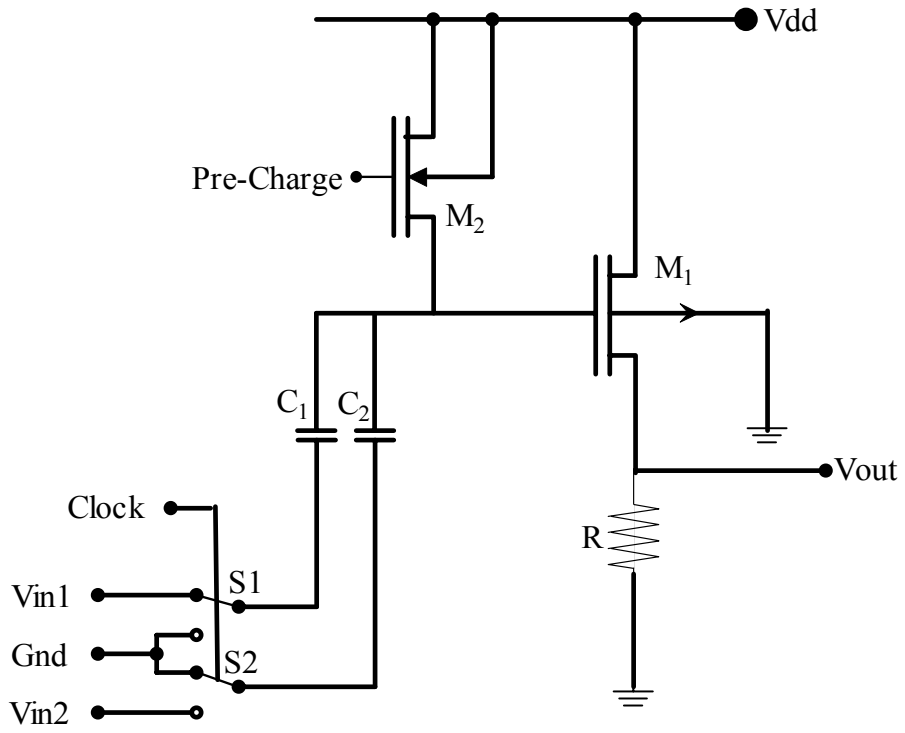

Figure 1.3. Circuit for the Principle of AC Nulling Technique.

Chapter 2. Floating Gate MOSFETs and Multiple-Input Floating Gate MOS Inverter

2.1 Basic Structure of a Floating Gate MOSFET

The basic structure of a floating gate MOSFET is shown in Figure 2.1 [14]. Arrays of control gates, which are inputs to the transistor, are formed over the floating gate using the second polysilicon layer [9, 15, 16]. The potential on the gate, Φ_f is primarily determined by the capacitance values of the input capacitors and the voltage applied to them and is given by [17, 18],

$$\phi_F = \frac{C_1V_1 + C_2V_2 + ... + C_nV_n}{C_{TOT}} = \frac{\sum_{i=1}^{n} C_iV_i}{\sum_{i=0}^{n} C_i} \tag{2.1}$$

where $C_{TOT} = \sum_{i=0}^{n} C_i$ and n represents the number of inputs.V_1, V_2, …,V_n are the input signal voltages and C_1, C_2, …, C_n are the capacitive coupling coefficients between the floating gate and the substrate. The net potential on the floating gate is determined as a linear sum of all input signals weighted by the capacitive coupling coefficient [18]. The voltage signals are directly added at the gate level as shown in equation (2.1). Here the substrate potential and floating gate charge are neglected for simplicity. For the transistor to turn on, Φ_f should exceed MOSFET threshold voltage, V_{TH} and vice versa. Hence the weighted sum of all the inputs determines the "on" and "off" state of the MOSFET.

2.2 I-V Characteristics of a Floating Gate n-MOSFET

The symbol representing an n-type FGMOSFET is shown in Figure 2.2 and the corresponding circuit to obtain its I-V characteristics is shown in Figure 2.3. A capacitor

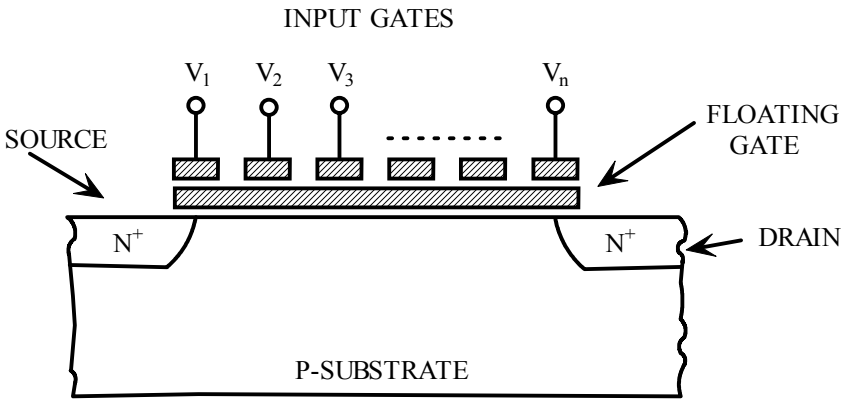

Figure 2.1. Floating Gate n-MOSFET

value of 250 fF which is also the unit capacitance is used as the gate input. DC analysis cannot be performed under normal circumstances [25, 26] because in SPICE the floating gate capacitor treats the DC voltage as an open source. Hence a large resistance is added between the floating gate node and ground. DC sweep can now be performed as shown in Figure 2.4 and Figure 2.5 and the transfer characteristics of an n-type floating gate MOSFET are obtained.

2.3 I-V Characteristics of a Floating Gate p-MOSFET

The symbol representing the floating gate p-MOSFET is shown in Figure 2.6[20] and the corresponding circuit to obtain its I-V characteristics is shown in Figure 2.7. A capacitance value of 250fF which is also the unit capacitance is coupled to the floating gate at its input. Contrary to the n-MOSFET the DC voltage source V_{DS} applied at the drain of the transistor is changed to a ramp voltage source (0 - 3 V) that would give same result as when DC analysis is performed and the circuit is simulated for various values of V_{GS}. Figures 2.8 and 2.9 show the transfer characteristics of the floating gate p-MOSFET.

2.4 Multiple-Input Floating Gate CMOS Inverter

A multiple input floating gate CMOS inverter is shown in Figure 2.10. V_1, V_2, V_3 … V_n are the input voltages and C_1, C_2, C_3… C_n are corresponding input capacitors. The voltage on the floating gate V_{in} is the multiple valued input voltage which is obtained by calculating the weighted sum of all inputs at the floating gate. The switching of the floating gate CMOS inverter is contingent on whether the V_{in} obtained from the weighted

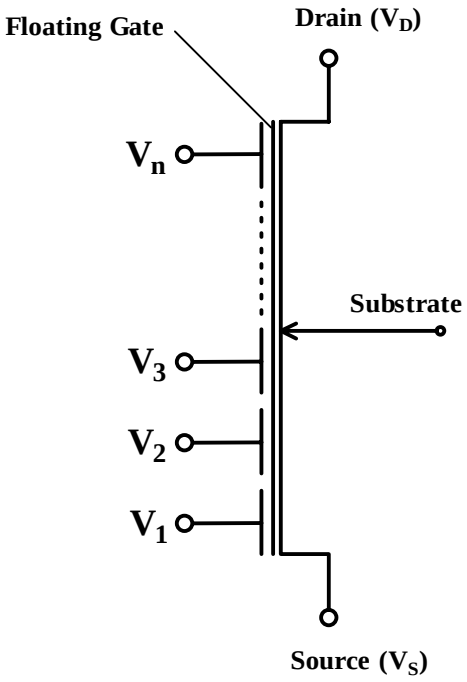

Figure 2.2. Symbol of a Multiple Input Floating Gate n-MOSFET.

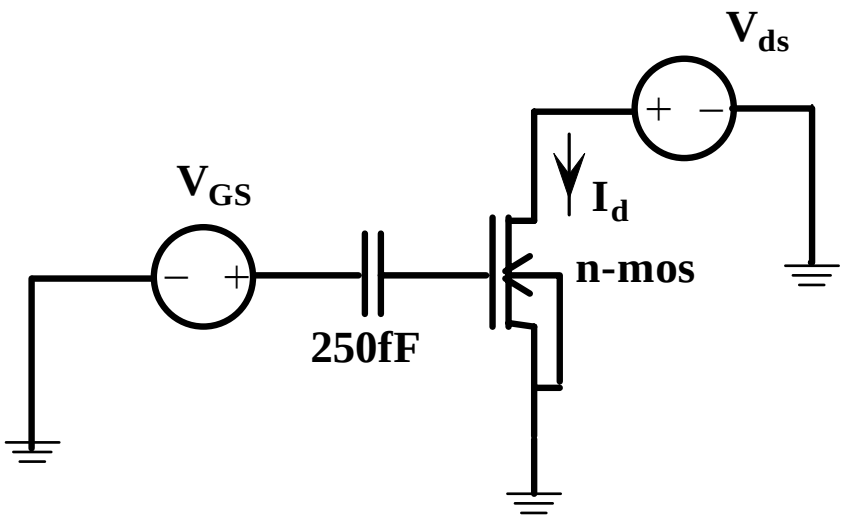

Figure 2.3. Circuit Diagram for I-V Characterization.

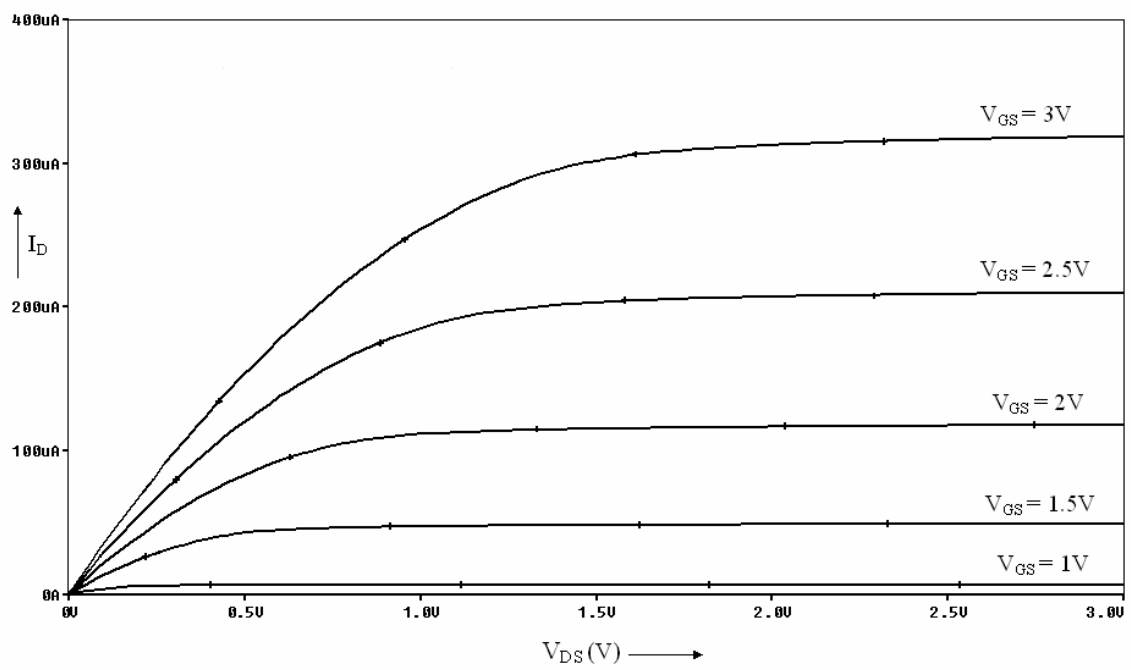

Figure 2.4. I-V Characteristics of Floating Gate n- MOSFET (W/L = 4.2/2.1).

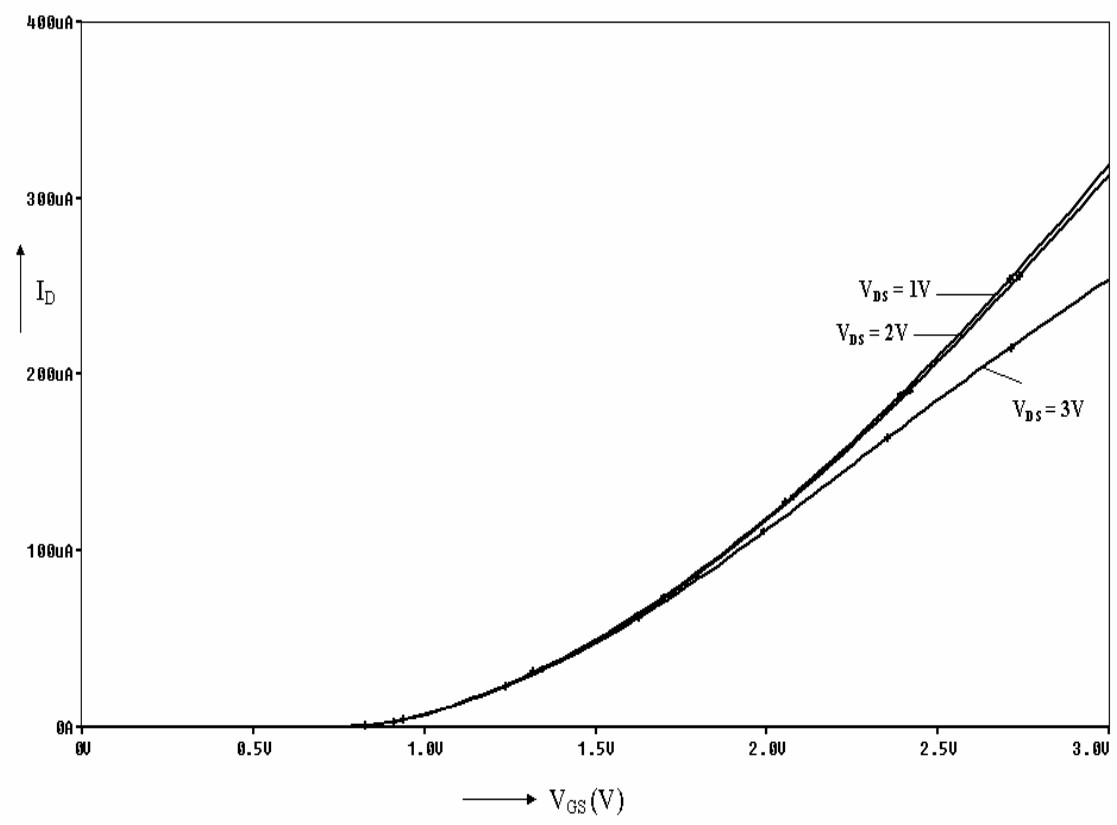

Figure 2.5.Transfer Characteristics of a Floating Gate n-MOSFET (W/L=4.2/2.1)

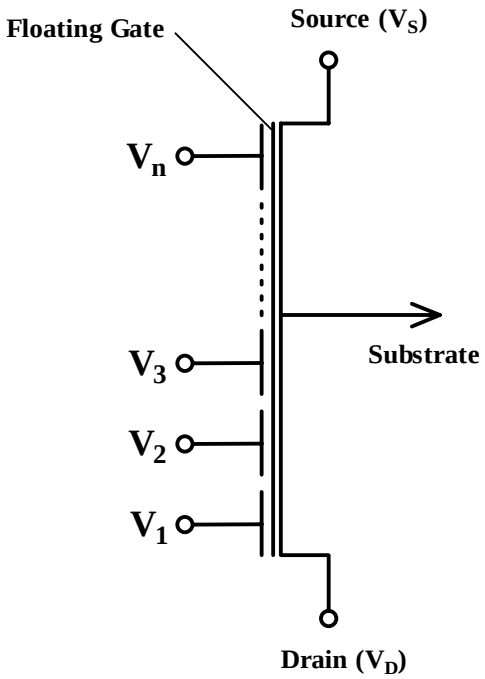

Figure 2.6. Symbol of a Multiple Input Floating Gate p-MOSFET.

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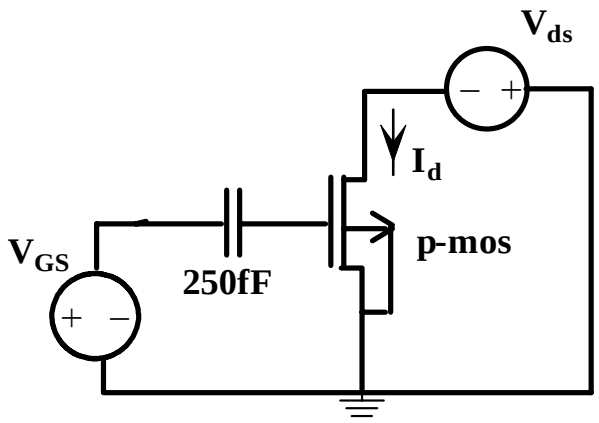


Figure 2.7. Circuit Diagram for the Transient Analysis of the Floating Gate p-MOSFET.

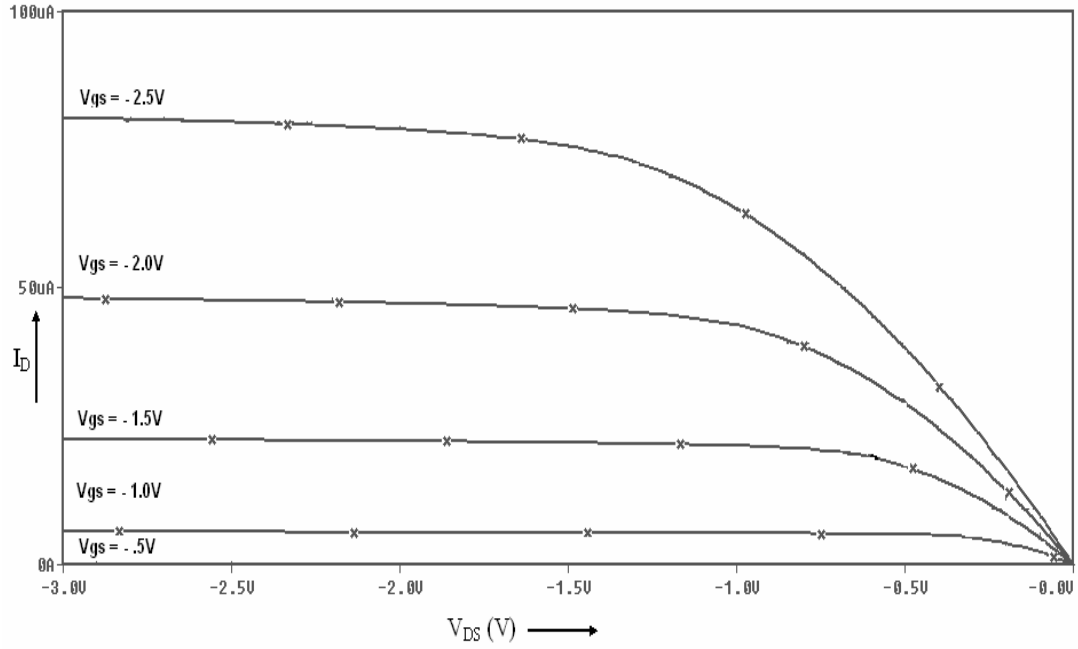


Figure 2.8. I-V Characteristics of a Floating Gate p-MOSFET (W/L = 4.2/2.1).

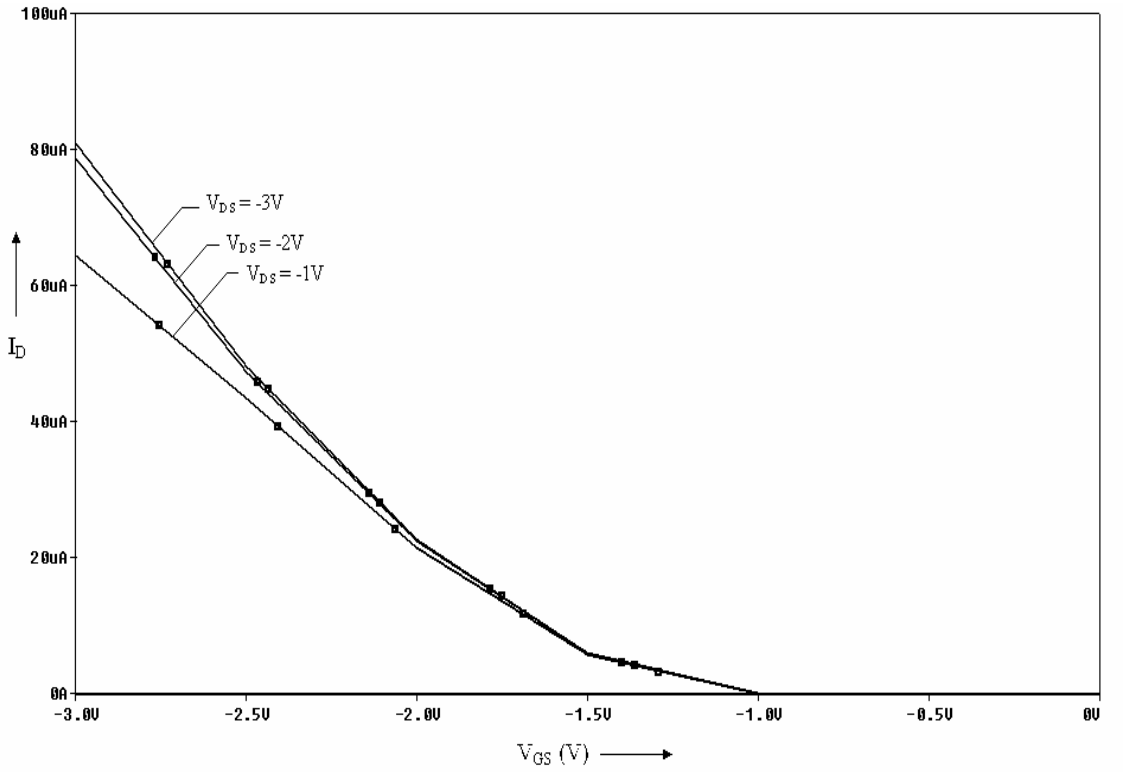


Figure 2.9. Transfer Characteristics of a Floating Gate p-MOSFET (W/L = 4.2/2.1).

sum, is greater than or less than the inverter threshold voltage or inverter switching voltage (Φ_t). The switching voltage is computed from the voltage transfer characteristics of a standard CMOS inverter and is given by the following equation [21, 22].

$$\phi_t = \frac{\phi_{g0} + \phi_{s1}}{2} \tag{2.2}$$

Where Φ_{g0} is the input voltage (0 V) at which the output voltage is V_{DD} - 0.1V which corresponds to an output of logic '1', and Φ_{s1} is the input voltage (3 V) at which the output voltage is 0.1V and corresponds to logic '0'. Hence, the output (V_{out}) of a multi-input floating gate CMOS inverter is [8]

V_{out} = HIGH (3 V) if $\Phi_{g0} < \Phi_{s1}$

= LOW (0 V) if $\Phi_{g0} > \Phi_{s1}$. (2.3)

Φ_{g0} and Φ_{s1} are obtained from the transfer characteristics of the CMOS inverter. The transfer characteristics along with the values for Φ_{g0} and Φ_{s1} are shown in Figure 2.11.

2.5 Variable Threshold Voltage

The novelty of the multiple-input floating gate inverter lies in the fact that the switching voltage can be varied by altering the values of the capacitors through which the inputs are coupled to the gate. Ordinarily, varying the W_p/W_n ratios of the inverter achieves the change in threshold voltage. In multiple-input floating gate inverters, varying the coupling capacitances to the gate can vary the switching point in DC transfer characteristics [24]. The voltage transfer characteristics of multiple-input floating gate CMOS inverters with varying W_p/W_n ratios and a constant L of 0.6 μm are shown in Figure 2.12.

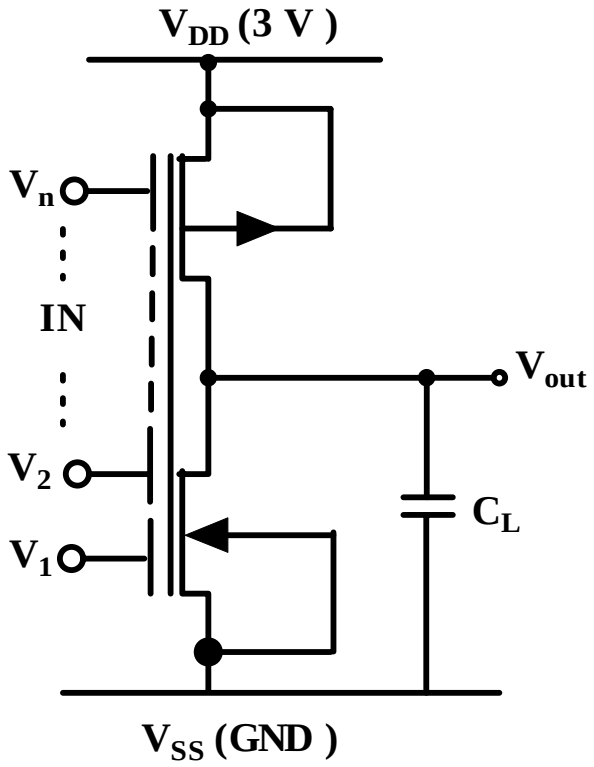


Figure 2.10. Multiple-Input Floating Gate CMOS Inverter.

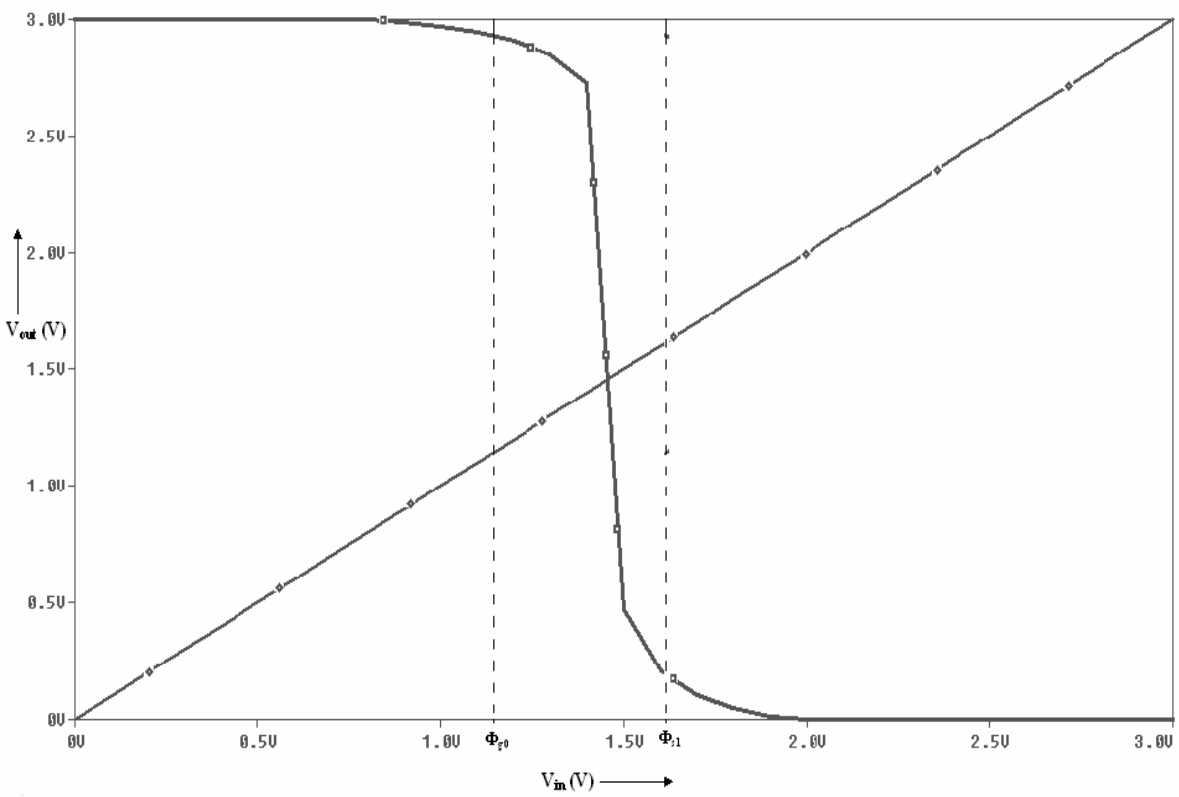


Figure 2.11. Transfer Characteristics of a Floating Gate CMOS Inverter.
Note: $\Phi_{g0} = 1.07$ V and $\Phi_{s1} = 1.59$ V. $(W/L)_p = 10.2/2.1$ and $(W/L)_n = 4.2/2.1$

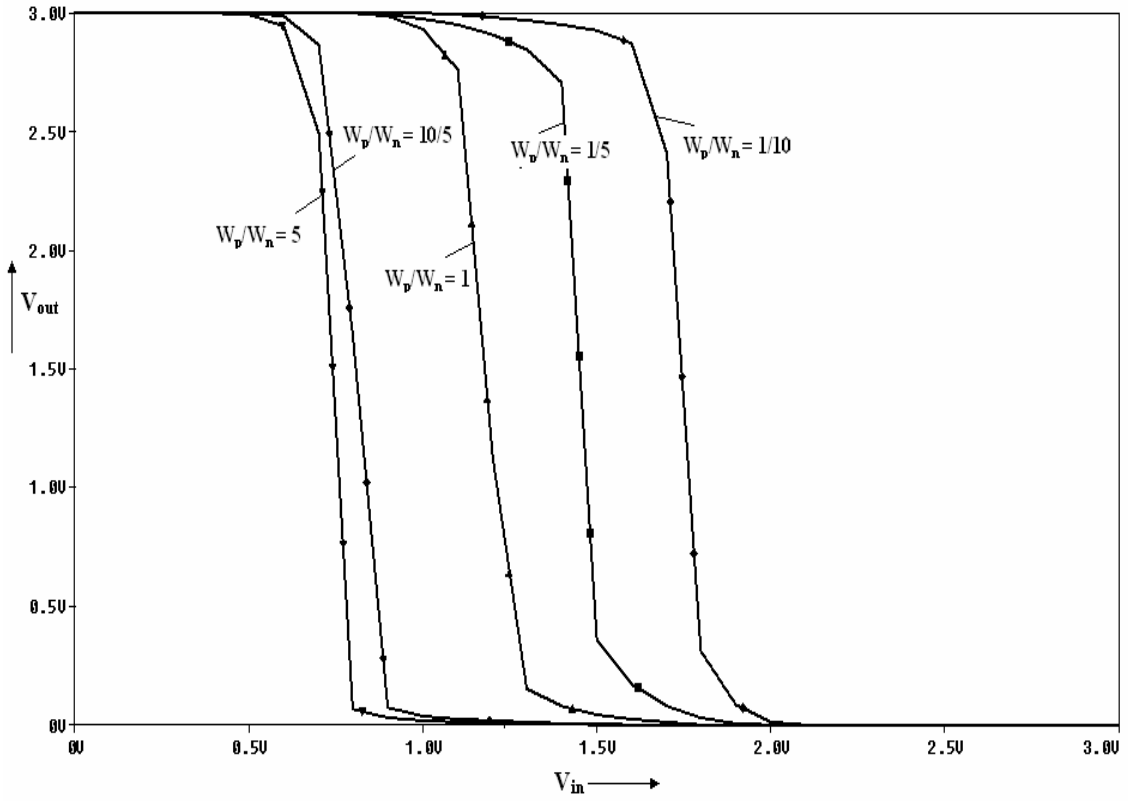


Figure 2.12. Transfer Characteristics of Floating Gate CMOS Inverter for Varying W_p/W_n Ratios.

Chapter 3. Design of Ternary to Binary Bit Converter

3.1 Introduction

Ternary logic system has advantages over the binary system in terms of circuit cost and complexity [27]. The balanced ternary logic can be expressed as -1, 0, 1 and can be implemented in a standard 3 V CMOS process. The logic -1, 0, 1 is represented as three voltage levels -3 V, 0 V, 3 V. Despite the afore mentioned advantages of ternary logic system, it has not gained importance in the area of IC design due to the lack of effective and efficient interfacing circuits with binary logic systems. This has been the primary motivation in attempting to design the ternary-to-binary converter. As an example the conversion of a decimal number "-2" for which the corresponding binary bits are $(1010)_2$ and the ternary bits are $(-1, 1)_3$ is shown below. The left most bit in the binary system i.e.,1, represents the sign bit and the next three bits 010 represent the number 2.

$$(-1 \times 3^1) + (1 \times 3^0) = (-3) + (1) = -2$$

$$-2 \equiv 1\ 0\ 1\ 0$$

The conversion from ternary-to-binary bits is summarized in Table 3.1 along with the decimal representation.In this chapter, the design of the conversion circuit from ternary logic to binary logic is presented. The two ternary inputs (MSB, LSB) are coupled capacitively to the floating gate through two capacitors and the four binary outputs are obtained in the form of sign bit (SB), most significant bit (MSB), second significant bit (SSB) and least significant bit (LSB).

Table 3.1. Decimal Number, Ternary and Binary Bits

Decimal	Ternary	Binary
-4	$(-1\ -1)_3$	$(1100)_2$
-3	$(-1\ \ 0)_3$	$(1011)_2$
-2	$(-1\ \ 1)_3$	$(1010)_2$
-1	$(\ 0\ -1)_3$	$(1001)_2$
0	$(\ 0\ \ 0)_3$	$(0000)_2$
1	$(\ 0\ \ 1)_3$	$(0001)_2$
2	$(\ 1\ -1)_3$	$(0010)_2$
3	$(\ 1\ \ 0)_3$	$(0011)_2$
4	$(\ 1\ \ 1)_3$	$(0100)_2$

Note: Ternary bits are represented as $(MSB, LSB)_3$, binary bits are represented as (Sign Bit, MSB, SSB, LSB)

3.2 Circuit Design for Sign Bit

The switching threshold voltage Φ_t is first calculated for an inverter with W/L ratio 20.35 μm / 2.1 μm (pMOS) and 4.2 μm / 2.1 μm (nMOS). This value is obtained from the voltage transfer characteristics of the inverter by performing DC analysis and extracting the values of Φ_{g0} and Φ_{s1} as shown in Figure 3.1. Φ_{g0} and Φ_{s1} are the input voltages at which the output of the inverter is V_{DD} - 0.1 V and 0.1 V, respectively and these are found to be 1.2094 V and 1.6806 V. Φ_t is computed by taking the average of Φ_{g0} and Φ_{s1} as shown in the equation below.

$$\phi_t = \left(\frac{\phi_{g0} + \phi_{s1}}{2} \right) = \frac{1.2094 + 1.6806}{2} = 1.445\,\mathrm{V} \tag{3.1}$$

The floating gate potential diagrams [28, 29] are drawn as the next step in designing these circuits as shown in Figure 3.3.

From Table 3.1, the sign bit is logic HIGH (3 V) for inputs $(-1, -1)_3$ to $(0, -1)_3$ and logic LOW (0 V) for inputs $(0, 0)_3$ to $(1, 1)_3$. The floating gate voltage Φ_f of the inverter should be below the switching voltage Φ_t for inputs $(-1, -1)_3$ to $(0, -1)_3$ and above switching voltage for inputs $(0, 0)_3$ to $(1, 1)_3$ [22]. The switching threshold line is marked in the floating gate potential diagram for the sign bit.

The circuit (stage #1) of the sign bit shown in Figure 3.2 is realized with two input capacitors C_1 and C_2 which are capacitively coupled to the floating gate and governed by the ternary inputs V_A and V_B, respectively.

The sizes of the capacitors are set in the ratio of 3:1 according to the weights of MSB and LSB in ternary bits. Using the following equations, we obtain [20, 8] for inputs

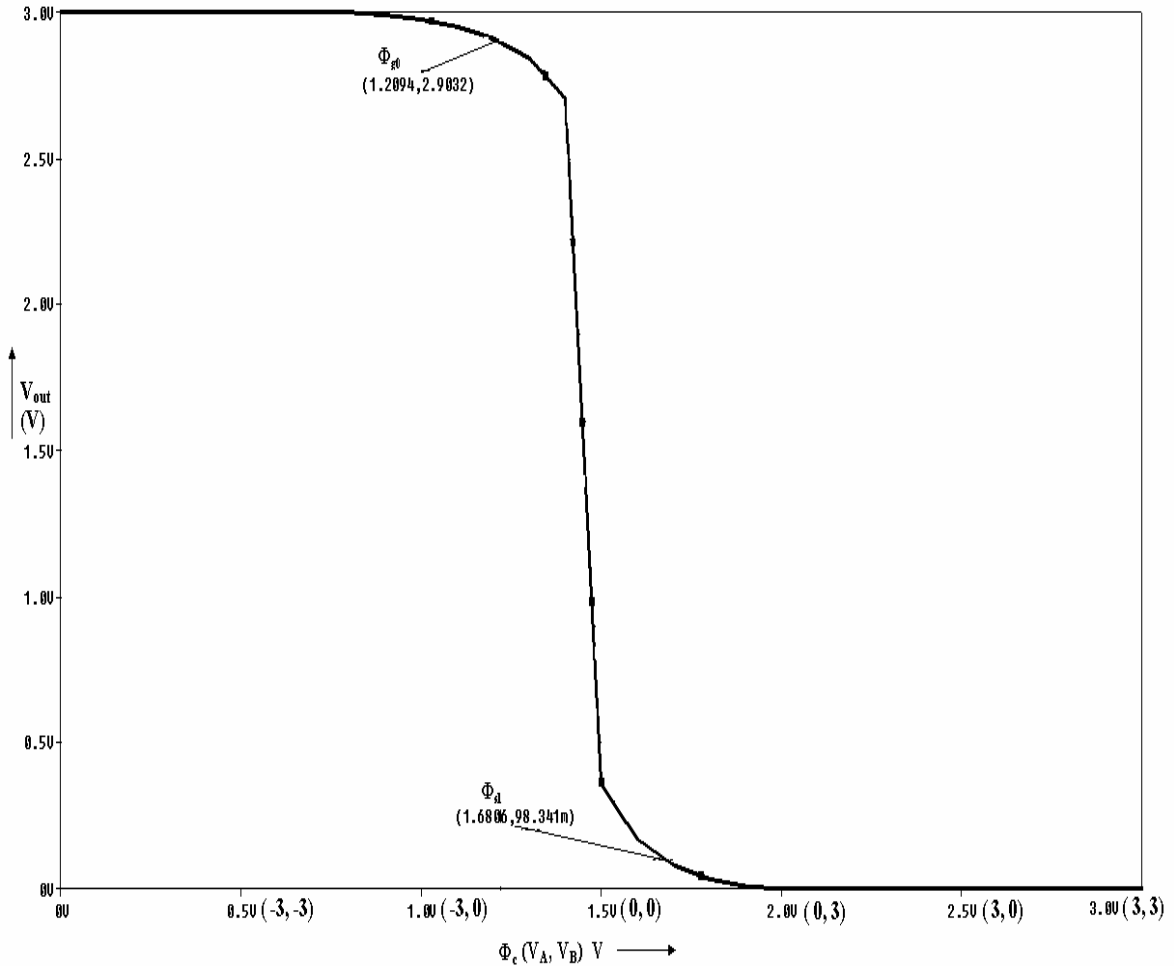


Figure 3.1. VTC of the SB-Circuit of Figure 3.3 to Calculate Φ_t.
Note: $V_C = V_{DD}$.

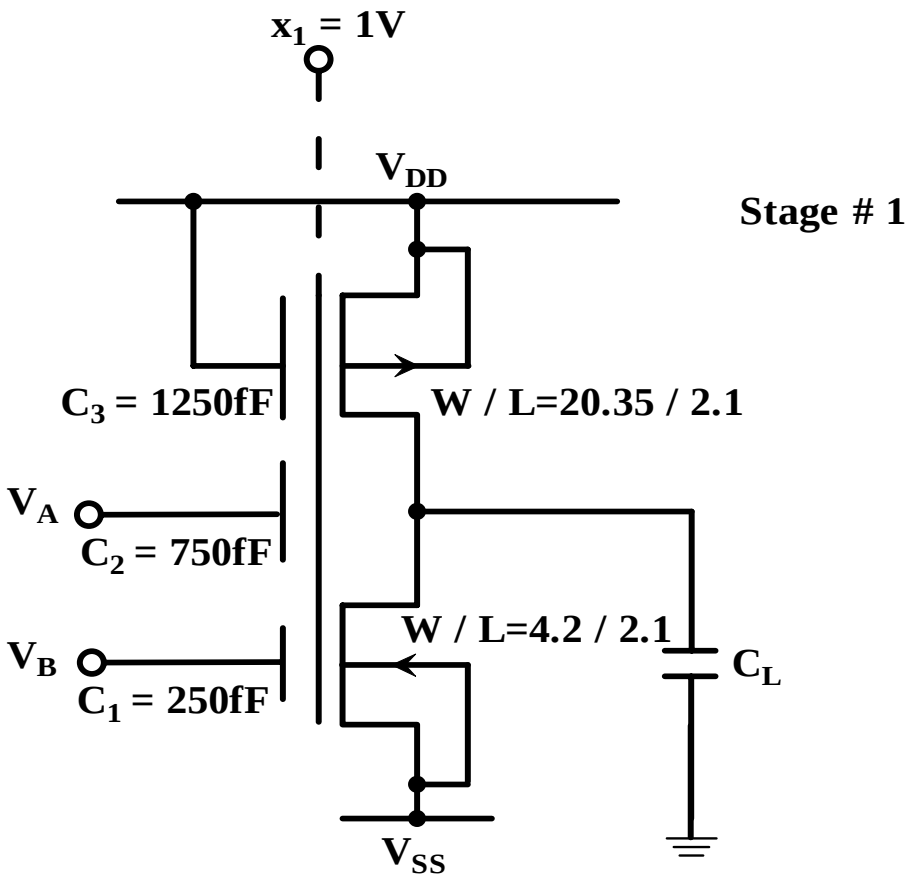


Figure 3.2 Circuit Diagram(Stage # 1) for Sign Bit (SB) Implementation.
Note: x_1 = 1V [equation (3.8)], V_{DD} = 3 V and V_{SS} = 0 V.

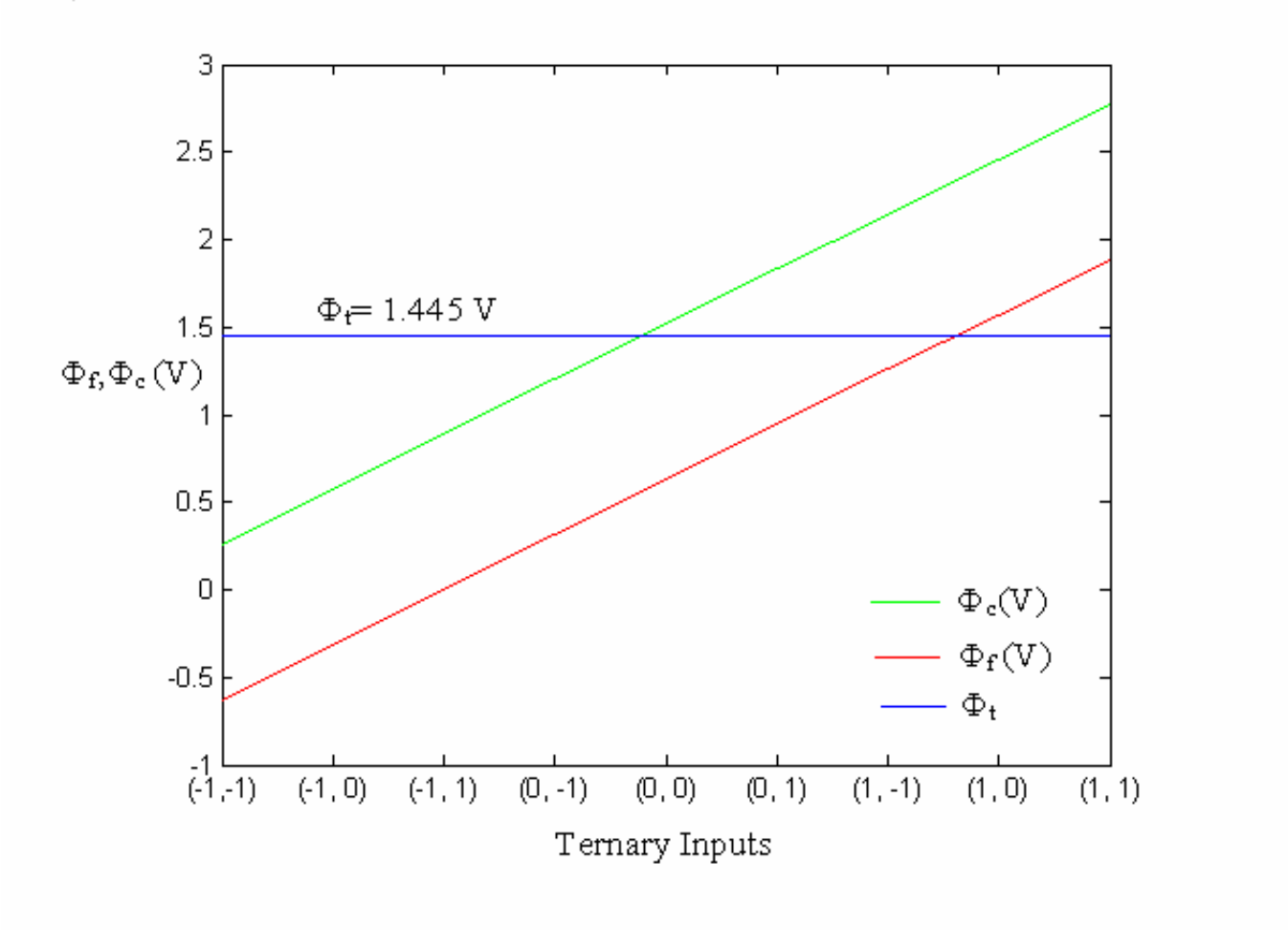


Figure 3.3. FPD of the SB-Circuit of Figure 3.2 (Stage # 1).

$(-1, -1)_3$ to $(0, -1)_3$,

$$\phi_F = \frac{V_A C_1 + V_B C_2 + V_{DD} C_{oxp}}{C_1 + C_2 + C_{oxp} + C_p + C_{oxn}} < \phi_t \tag{3.2}$$

and for inputs $(0, 0)_3$ to $(1, 1)_3$,

$$\phi_F = \frac{V_A C_1 + V_B C_2 + V_{DD} C_{oxp}}{C_1 + C_2 + C_{oxp} + C_p + C_{oxn}} > \phi_t \tag{3.3}$$

where C_p is the parasitic capacitance due to capacitors C_1 and C_2. C_{oxn} and C_{oxp} are the gate oxide capacitance (C_{ox}) of n-MOS and p-MOS transistors, respectively. C_{ox} is given by,

$$C_{ox} = \frac{\in_0 \in_{SiO_2}}{t_{ox}} \times (WL) \tag{3.4}$$

where $\in_0 = 8.854 \times 10^{-12} F/m$ is the permittivity of free space, $\in_{SiO_2} = 3.8$, is the permittivity of silicon dioxide, t_{ox} is the thickness of gate oxide, and W and L are the width and length of the transistor.

A unit capacitance C of 250 fF is chosen after considering the influence of parasitic capacitances. The values of capacitors C_1 and C_2 are set to 250 fF and 750 fF, respectively, in the ratio of 1:3. For the input $(0, 0)_3$, the equation (3.3) is not satisfied. Hence a third capacitance C_3 is introduced which is connected to the supply voltage. The size of the third capacitor is designed such that the voltage on the floating gate satisfies equation (3.3) as shown below.

$$\phi_F = \frac{V_A C_1 + V_B C_2 + V_{DD} C_3 + V_{DD} C_{oxp}}{C_1 + C_2 + C_3 + C_{oxp} + C_p + C_{oxn}} > \phi_t \tag{3.5}$$

The parasitic capacitance C_p for equation 3.5 is calculated as follows.

$$C_p = k \times C_{p1}$$

where C_{p1} is the parasitic capacitance generated by the unit capacitance of 250 fF and k is given by [8,19],

$$k = \frac{C_1 + C_2 + C_3}{C} \tag{3.6}$$

The calculated C_p is 15 fF. C_{oxn} and C_{oxp} are calculated from equation (3.4). Substituting the values of C_p, C_{oxp} and C_{oxn} in equation (3.5), the minimum value of C_3 which satisfies the equation is

$$C_3 > 956.7\, fF\ .$$

Expressing C_3 in integer multiple of a unit capacitor, C_3 is set at 1250 fF. This value for the capacitance is also verified by substituting it in the inequality for other inputs. The results are given in Table 3.2. From Table 3.2 it is noted that for inputs $(0, 0)_3$, $(0, 1)_3$ and $(1, -1)_3$, the equation is not satisfied and is also shown in the FPD of the SB-circuit of Figure 3.2.

From the floating point diagram shown in Figure 3.3 we notice that Φ_f deviates from the threshold voltage Φ_t(1.445V). The average (x_1 V) of these deviations is computed using the following equation (3.7) [30],

$$x_1 = \sqrt{\frac{1}{n-1}\left(\sum_{i=1}^{n}(d_i)^2\right)} \tag{3.7}$$

where n is the total combination of ternary inputs and is equal to 9, and d_i is the deviation of Φ_f from Φ_t for each input. For the SB, x_1 is 0.896 V and is approximated to 1 V. Φ_f is corrected using the x obtained from equation (3.7) in order to obtain the correct output (Table 3.2) as shown in equation (3.8).

Table 3.2. Gate Voltages for Ternary Inputs of Stage #1of SB With and Without Bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.445V)	Binary Output	Expected Output	Φ_c (V) ($\Phi_f \pm x$) x_1=1V	Φ_c vs. Φ_t (Φ_t=1.445V)
(-1, -1)	-0.634	$\Phi_f < \Phi_t$	1	1	0.367	$\Phi_c < \Phi_t$
(-1, 0)	-0.317	$\Phi_f < \Phi_t$	1	1	0.684	$\Phi_c < \Phi_t$
(-1, 1)	-0.0012	$\Phi_f < \Phi_t$	1	1	1	$\Phi_c < \Phi_t$
(0, -1)	0.315	$\Phi_f < \Phi_t$	1	1	1.31	$\Phi_c < \Phi_t$
(0, 0)	0.632	$\Phi_f < \Phi_t$	1	0	1.62	$\Phi_c > \Phi_t$
(0, 1)	0.948	$\Phi_f < \Phi_t$	1	0	1.94	$\Phi_c > \Phi_t$
(1, -1)	1.26	$\Phi_f < \Phi_t$	1	0	2.25	$\Phi_c > \Phi_t$
(1, 0)	1.57	$\Phi_f > \Phi_t$	0	0	2.58	$\Phi_c > \Phi_t$
(1, 1)	1.884	$\Phi_f > \Phi_t$	0	0	2.91	$\Phi_c > \Phi_t$

$$\phi_f \pm x_1 = \phi_c \tag{3.8}$$

where Φ_c is the resultant new floating gate potential. The values of Φ_c are computed for different values of inputs and are also shown in Table 3.2 and Figure 3.3. We notice from Figure 3.3 that the output which was in error for the previous gate value at inputs $(0, 0)_3$, $(0, 1)_3$ and $(1, -1)_3$ has been now corrected. The equation (3.5) is now satisfied for all values of ternary inputs with the value of C_3 set at 1250 fF. The floating gate in the SB-circuit of Figure 3.2 is biased at fixed 1V, according to equation (3.8).

3.3 Circuit Design for Most Significant Bit (MSB)

From Table 3.1, the MSB is found to be logic HIGH (3 V) for inputs $(-1, -1)_3$ and $(1, 1)_3$ and logic LOW for the rest of the inputs. The potential on the floating gate should be below the switching threshold voltage Φ_t for inputs $(-1, -1)_3$, $(1, 1)_3$ and above the switching threshold voltage for inputs $(-1, 0)_3$ to $(1, 0)_3$. The voltage on the floating gate switches above and below the threshold voltage only once and hence requires one pre-input gate inverter (stage #2) to control the voltage on floating gate of the stage #3 of the MSB as shown in Figure 3.4. The stage #3 of the MSB has three input capacitors C_6, C_7 and C_8. C_6, C_7 are controlled by ternary inputs V_A and V_B, respectively and C_8 by the output (V_2) from the pre-input gate inverter (stage #2).

DC analysis for the two inverters used in the design of the MSB is performed and the threshold voltage Φ_t for the pre-input gate inverter stage #2 and the stage #3 of the MSB are computed. The VTC (voltage transfer characteristics) is shown in Figure 3.5. The computed value of Φ_t is 1.54V.

MSB design equations are as follows [8].

For input $(-1, -1)_3$

$$\phi_F = \frac{(-3V)C_6 + (-3V)C_7 + V_2C_8 + V_{DD}C_{oxp}}{C_6 + C_7 + C_8 + C_{oxp} + C_p + C_{oxn}} < \phi_t \tag{3.9}$$

and for $(1, 1)_3$

$$\phi_F = \frac{(3V)C_6 + (3V)C_7 + V_2C_8 + V_{DD}C_{oxp}}{C_6 + C_7 + C_8 + C_{oxp} + C_p + C_{oxn}} < \phi_t \tag{3.10}$$

Equations (3.9) and (3.10) can be satisfied only if V_2 in Figure 3.4 is LOW (0 V) for input $(1, 1)_3$ and HIGH (3 V) for rest of the inputs according to Table 3.1. In Figure 3.4, the value of capacitors C_6 and C_7 are set in the ratio 1:1. So the minimum size of capacitor C_6 and C_7 are set at 250 fF and 250 fF, respectively. The value of C_8 is 1250 fF which satisfies equations (3.9) and (3.10). Figure 3.6 shows the resulting FPD of the MSB. Table 3.3 summarizes Φ_f, Φ_f versus Φ_t, binary output and expected binary output for all combinations of ternary inputs following the FPD of the MSB {Figure (3.6)}. It may be inferred that the outputs for inputs $(-1, 0)_3$ to $(1, 0)_3$ do not conform with the expected output because the floating gate potential $\Phi_f < \Phi_t$, where $\Phi_f > \Phi_t$. The average value (x_3 V) of deviations with respect to Φ_t which is 1.45V is computed. This average value x_3 =1.45 is appended to the gate potential Φ_f to give the new floating gate potential, Φ_c as shown in Figure 3.6. We notice from Figure 3.6 that the output which was incorrect at inputs $(-1, 0)_3$ to $(1, 0)_3$ is now in agreement with the expected outputs.

3.3.1 Circuit Design for Pre-input Inverter Stage #2

The first step in the design of the pre-input inverter stage is to determine the threshold voltage Φ_t for the W/L values of the pMOS (30.15 μm / 2.1 μm) and nMOS (4.2 μm / 2.1 μm) transistors used in constructing the CMOS inverter. The value of Φ_{g0} and Φ_{s1} needed to compute Φ_t can be extracted from the DC transfer characteristics of the inverter and is

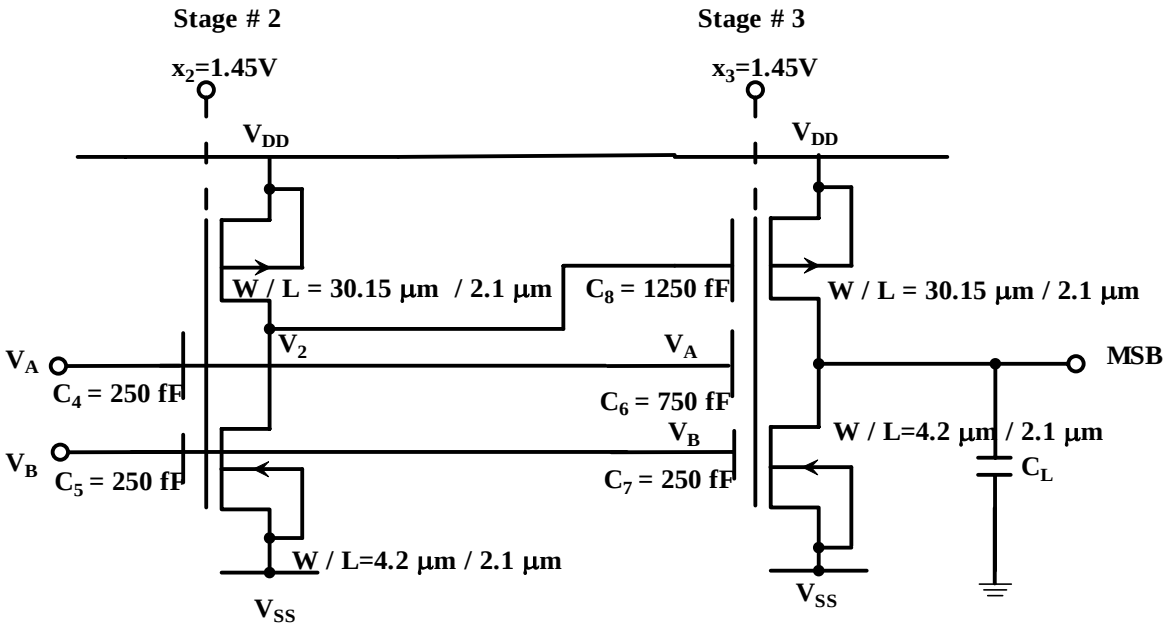


Figure 3.4 Circuit Diagram of Most Significant Bit (MSB) Implementation.
Note: V_{DD} = 3 V and V_{SS} = 0 V.

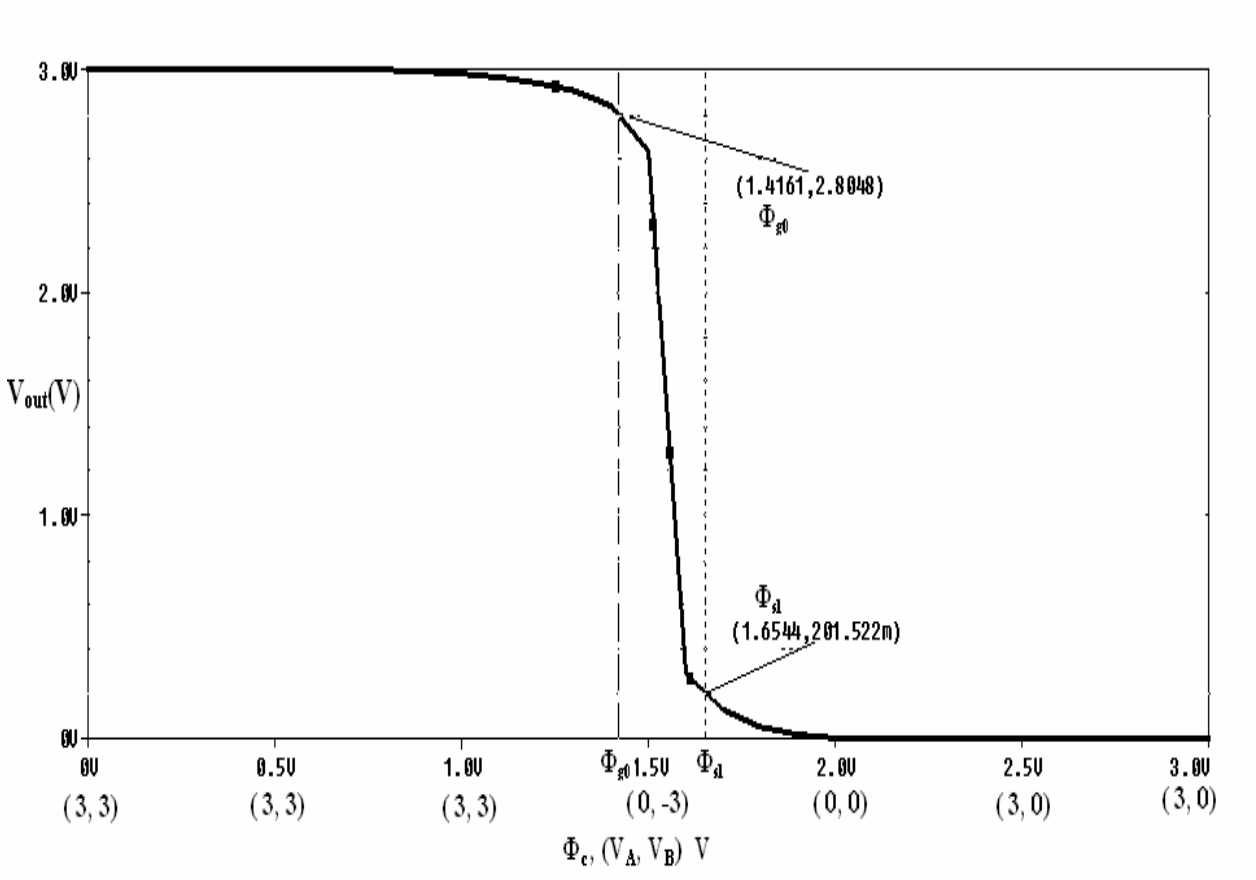


Figure 3.5. VTC of the MSB (Stage # 3) Circuit of Figure 3.4 to calculate Φ_t.

the same as shown in Figure 3.5 since W/L values of transistors are identical. The Φ_t is 1.54V as computed earlier. The output of stage #2 is LOW (0 V) for $(1, 1)_3$ and HIGH (3 V) for rest of the inputs. This circuit can be designed using two input capacitors C_4 and C_5. For input $(1, 1)_3$, the design conditions are [8], $\phi_F = \dfrac{V_A C_4 + V_B C_5 + V_{DD} C_{oxp}}{C_4 + C_5 + C_{oxp} + C_p + C_{oxn}} > \phi_t$

$$\phi_F = \frac{(3V)C_4 + (3V)C_5 + (3V)C_{oxp}}{C_4 + C_5 + C_{oxp} + C_p + C_{oxn}} > \phi_t \tag{3.11}$$

The capacitors C_4 and C_5 are equal and set to 250 fF each, which is the value of unit capacitance in order to satisfy above equations. The voltage Φ_f on the floating gate is calculated for different ternary inputs as shown in Figure 3.7 for FPD. The value of Φ_t is also shown in the FPD. The output of this stage controls the input capacitor C_8 of the stage #3 as shown in Figure 3.4.

To obtain the correct output at the main inverter stage, the gate voltage of the pre-input inverter stage needs to be modulated. From the FPD for the pre-input gate inverter stage (#2) we notice that the floating gate potential Φ_f deviates from the threshold voltage Φ_t. The average (x_2 V) of these deviations is computed and added to Φ_f to get the modulated or biased gate potential Φ_c. The value of x_2 was calculated to be 1.45 V. The gate potential Φ_c is calculated for different values of the input and is plotted as an FPD in Figure 3.7. The values of Φ_f and Φ_c for different ternary inputs and their comparison with Φ_t in order to get the expected output are tabulated in Table 3.4. From the table we notice that the output is in error for the input $(1, 1)_3$ and is corrected after gate modulation.

Table 3.3. Gate Voltages for Ternary Inputs of MSB Stage #3 With and Without Bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.54V)	Binary Output	Expected Output	Φ_c (V) $\Phi_f \pm x_3$ x_3=1.45V	Φ_c vs. Φ_t (Φ_t=1.54V)
(-1, -1)	-0.1556	$\Phi_f < \Phi_t$	1	1	1.299	$\Phi_c < \Phi_t$
(-1, 0)	0.212	$\Phi_f < \Phi_t$	1	0	1.65	$\Phi_c > \Phi_t$
(-1, 1)	0.58	$\Phi_f < \Phi_t$	1	0	2.02	$\Phi_c > \Phi_t$
(0, -1)	0.212	$\Phi_f < \Phi_t$	1	0	1.65	$\Phi_c > \Phi_t$
(0, 0)	0.579	$\Phi_f < \Phi_t$	1	0	2.02	$\Phi_c > \Phi_t$
(0, 1)	0.787	$\Phi_f < \Phi_t$	1	0	2.24	$\Phi_c > \Phi_t$
(1, -1)	0.579	$\Phi_f < \Phi_t$	1	0	2.02	$\Phi_c > \Phi_t$
(1, 0)	0.785	$\Phi_f < \Phi_t$	1	0	2.24	$\Phi_c > \Phi_t$
(1, 1)	-0.519	$\Phi_f < \Phi_t$	1	1	0.94	$\Phi_c < \Phi_t$

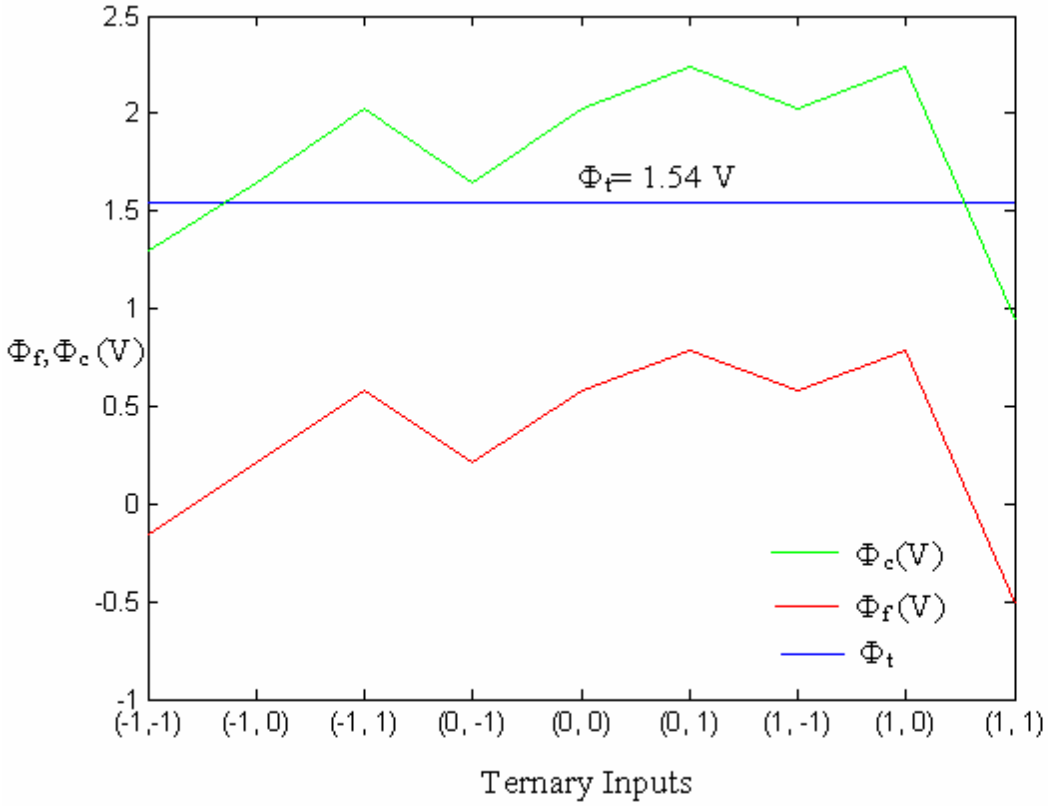


Figure 3.6. FPD of the MSB Circuit (Stage # 3) of Figure 3.4.

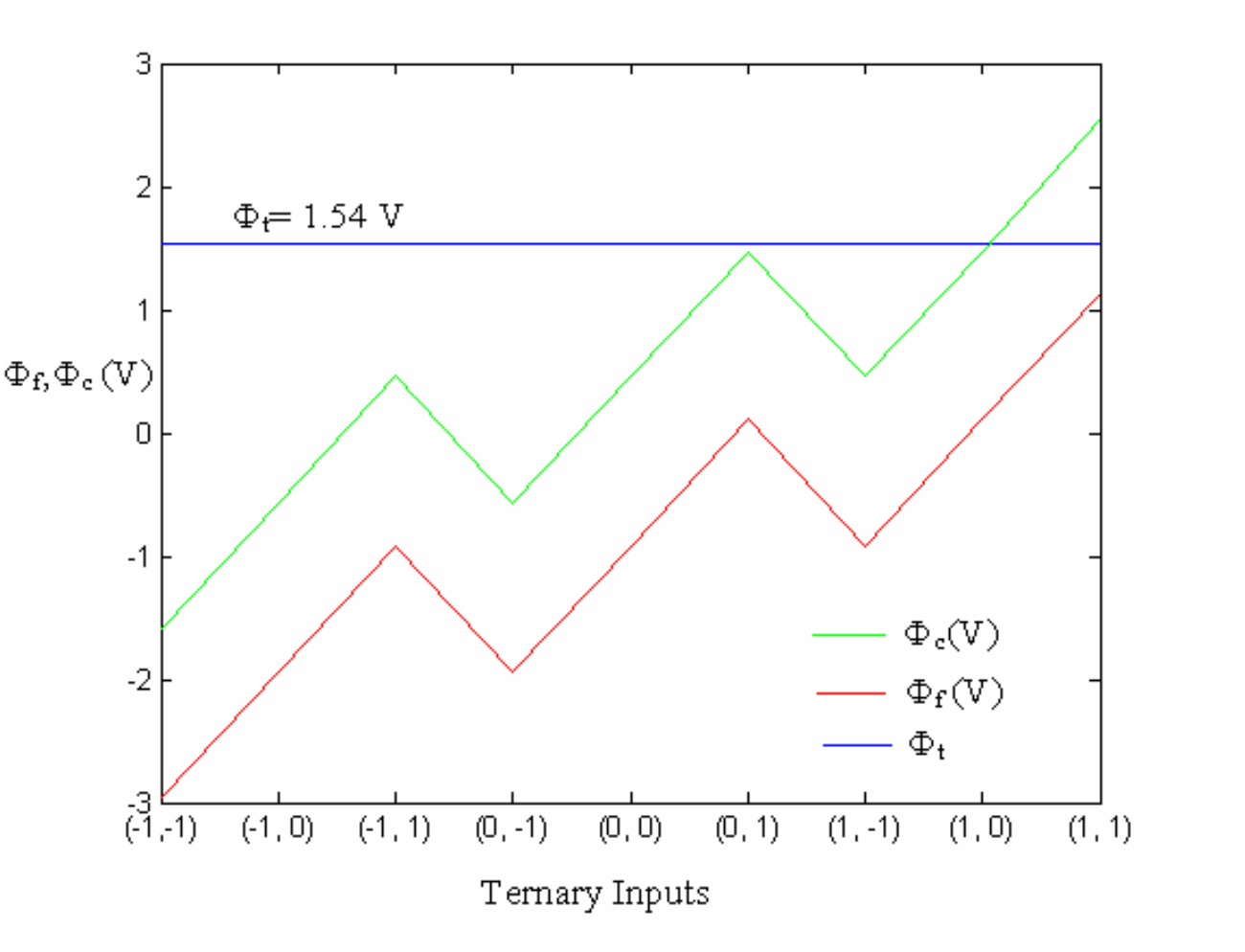


Figure 3.7. FPD of the Stage #2 of the MSB Circuit of Figure 3.4.
Note: x_2 = 1.45V.

Table 3.4. Gate Voltages for Ternary Inputs of MSB Pre-Input Gate Inverter Stage #2 With and Without Bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.54V)	Binary Output	Expected Output	Φ_c (V) $\Phi_f \pm x$ x_2=1.45V	Φ_c vs. Φ_t (Φ_t=1.54V)
(-1, -1)	-2.9632	$\Phi_f < \Phi_t$	1	1	-1.592	$\Phi_c < \Phi_t$
(-1, 0)	-1.944	$\Phi_f < \Phi_t$	1	1	-0.569	$\Phi_c < \Phi_t$
(-1, 1)	-0.923	$\Phi_f < \Phi_t$	1	1	0.464	$\Phi_c < \Phi_t$
(0, -1)	-1.944	$\Phi_f < \Phi_t$	1	1	-0.57	$\Phi_c < \Phi_t$
(0, 0)	-0.924	$\Phi_f < \Phi_t$	1	1	0.464	$\Phi_c < \Phi_t$
(0, 1)	0.107	$\Phi_f < \Phi_t$	1	1	1.47	$\Phi_c < \Phi_t$
(1, -1)	-0.924	$\Phi_f < \Phi_t$	1	1	0.463	$\Phi_c < \Phi_t$
(1, 0)	0.107	$\Phi_f < \Phi_t$	1	1	1.47	$\Phi_c < \Phi_t$
(1, 1)	1.133	$\Phi_f < \Phi_t$	1	0	2.56	$\Phi_c > \Phi_t$

3.4 Circuit Design for Secondary Significant Bit (SSB)

From Table 3.1, the output of the SSB is LOW (0 V) for inputs $(-1, -1)_3$,$(1, 1)_3$ and from inputs $(0, -1)_3$ to $(0, 1)_3$ and is logic HIGH (3 V) for the rest of the inputs. The first step in the design of the SSB is to calculate the threshold voltage Φ_t of the floating gate inverter used. The voltage on the floating gate goes above the switching threshold voltage for inputs $(-1, -1)_3$, $(1, 1)_3$ and for inputs from $(0, -1)_3$ to $(0, 1)_3$. The voltage on the floating gate falls below switching threshold voltage twice and hence two pre-input gate inverter stages #4 and #5 are required to control the voltage on the floating gate of stage #6 as shown in Figure 3.8. The output inverter stage #6 has two input capacitors C_{12}, C_{13} with inputs V_A and V_B and two other capacitors C_{14} and C_{15} which are controlled by the output V_4 and V_5 of the pre-inverter stages #4 and #5, respectively. The output V_4 of stage #4 goes LOW (0 V) from inputs $(0, -1)_3$ to $(1, 1)_3$ and the output V_5, of stage #5 goes LOW (0 V) for input $(1, 1)_3$ [8].

For the main inverter stage #6, the design equation for input $(-1, -1)_3$ is,

$$\phi_F = \frac{(-3V)C_{12} + (-3V)C_{13} + (3V)C_{14} + (3V)C_{15} + V_{DD}C_{oxp}}{C_{12} + C_{13} + C_{14} + C_{15} + C_{oxp} + C_p + C_{oxn}} < \phi_t . \tag{3.12}$$

For inputs $(-1, 0)_3$ and $(-1, 1)_3$ the design equation is,

$$\phi_F = \frac{V_A C_{12} + V_B C_{13} + (3V)C_{14} + (3V)C_{15} + V_{DD}C_{oxp}}{C_{12} + C_{13} + C_{14} + C_{15} + C_{oxp} + C_p + C_{oxn}} > \phi_t . \tag{3.13}$$

The output of stage #4 goes LOW (0 V) for inputs $(0, -1)_3$ to $(1, 1)_3$ and hence the governing equation is,

$$\phi_F = \frac{V_A C_{12} + V_B C_{13} + (0V)C_{14} + (3V)C_{15} + V_{DD}C_{oxp}}{C_{12} + C_{13} + C_{14} + C_{15} + C_{oxp} + C_p + C_{oxn}} < \phi_t . \tag{3.14}$$

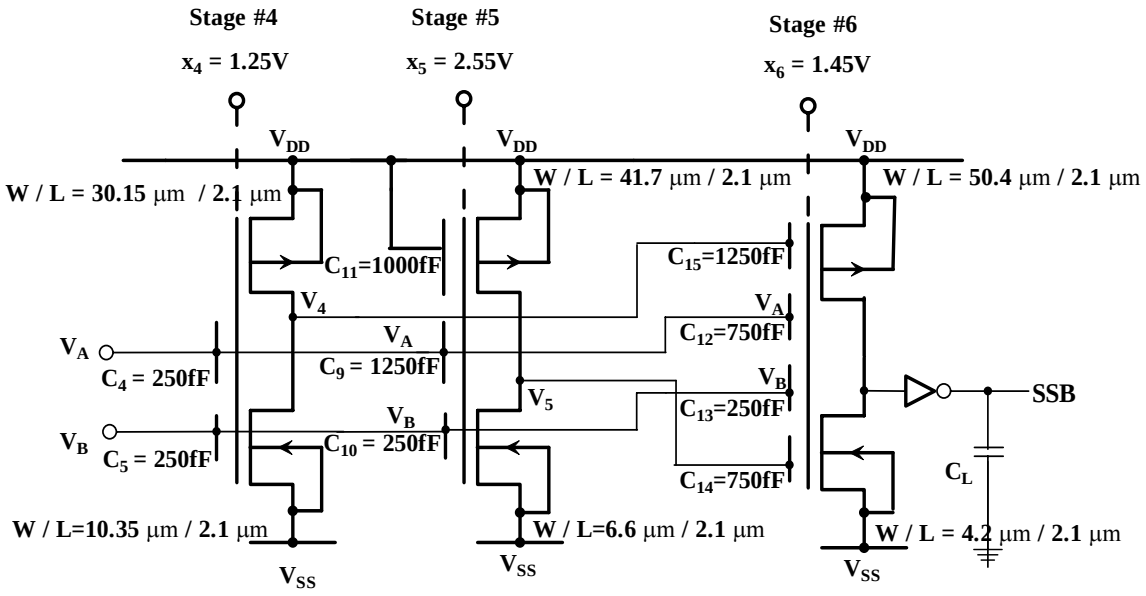


Figure 3.8. Circuit Diagram of Second Significant Bit (SSB) Implementation. Note: V_{DD} = 3 V and V_{SS} = 0 V.

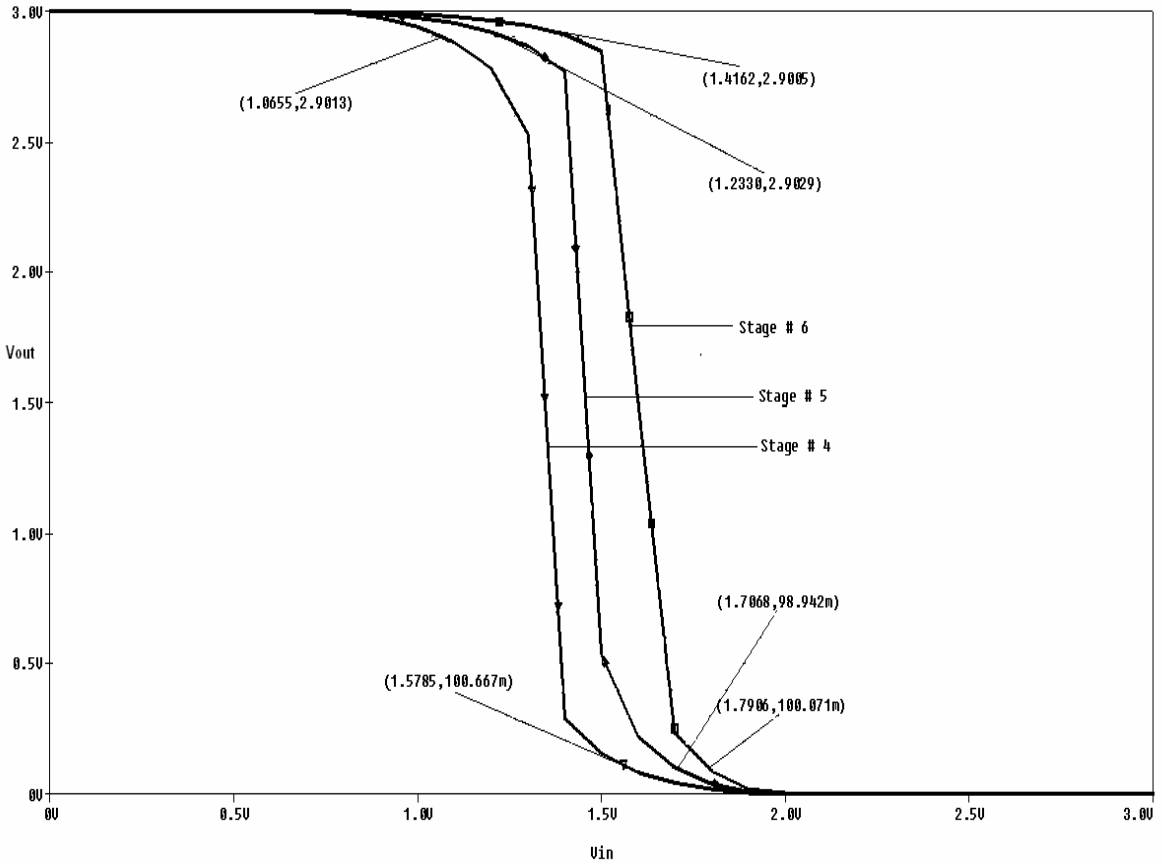


Figure 3.9. VTC of the Circuit of Figure 3.8.

Note: VTC for all the three stages of the SSB circuit of Figure 3.8 are shown. The x coordinates of the points in the upper half of the curves represent the Φ_{g0} and the x coordinates of the points in the lower half represent Φ_{s1} of the respective curves for the three stages of the SSB.

The value of Φ_t can be calculated by plotting the DC transfer characteristics for the inverter stage #6 shown in Figure 3.9. Φ_t is calculated by taking the average of Φ_{g0} and Φ_{s1} which are obtained for a W/L 50.4 μm / 2.1 μm for p-MOS and 4.2 μm / 2.1 μm for n-MOS transistors. The computed Φ_t for stage #6 is 1.6V. Substituting Φ_t in equations 3.12 to 3.14, C_{12}, C_{13}, C_{14} and C_{15} are obtained. Their values are 750 fF, 250 fF, 750 fF and 1250 fF, respectively. Figure 3.10 shows the FPD of the stage #6.

The biasing technique as described in earlier sections is employed to determine the modulated gate voltage after biasing the floating gate potential Φ_f to obtain the correct output. The FPD for the stage #6 showing the floating gate potential after biasing Φ_c for different ternary inputs is also shown in Figure 3.10. The computed x_6 is 1.45 V. The values of Φ_f and Φ_c are given in Table 3.5 and compared with Φ_t to obtain the correct output. The output of the inverter stage #6 is passed though another inverter to obtain the SSB. Hence in Table 3.5, the expected output is the complement of the SSB.

3.4.1 Circuit Design for Pre-Input Gate Inverter Stage #4 for SSB

The output of stage #4, V_4, goes LOW (0 V) from inputs $(1, 1)_3$ and stays HIGH (3 V) for the rest of the inputs. This stage requires 2 input capacitors C_4, and C_5 (which is the same as in stage #2 of MSB) which have inputs V_A and V_B respectively. The threshold voltage can be calculated from Figure 3.9 and is found to be Φ_t=1.33 V for a W/L of 30.15 μm / 2.1 μm for p-MOS and 10.35 μm / 2.1 μm for the n-MOS transistors. Using design equations for the stage #2 of MSB bit, the values of the capacitors are 250fF each and are same as the unit capacitance. The FPD for stage #4 showing Φ_f for different inputs is shown in Figure 3.11.

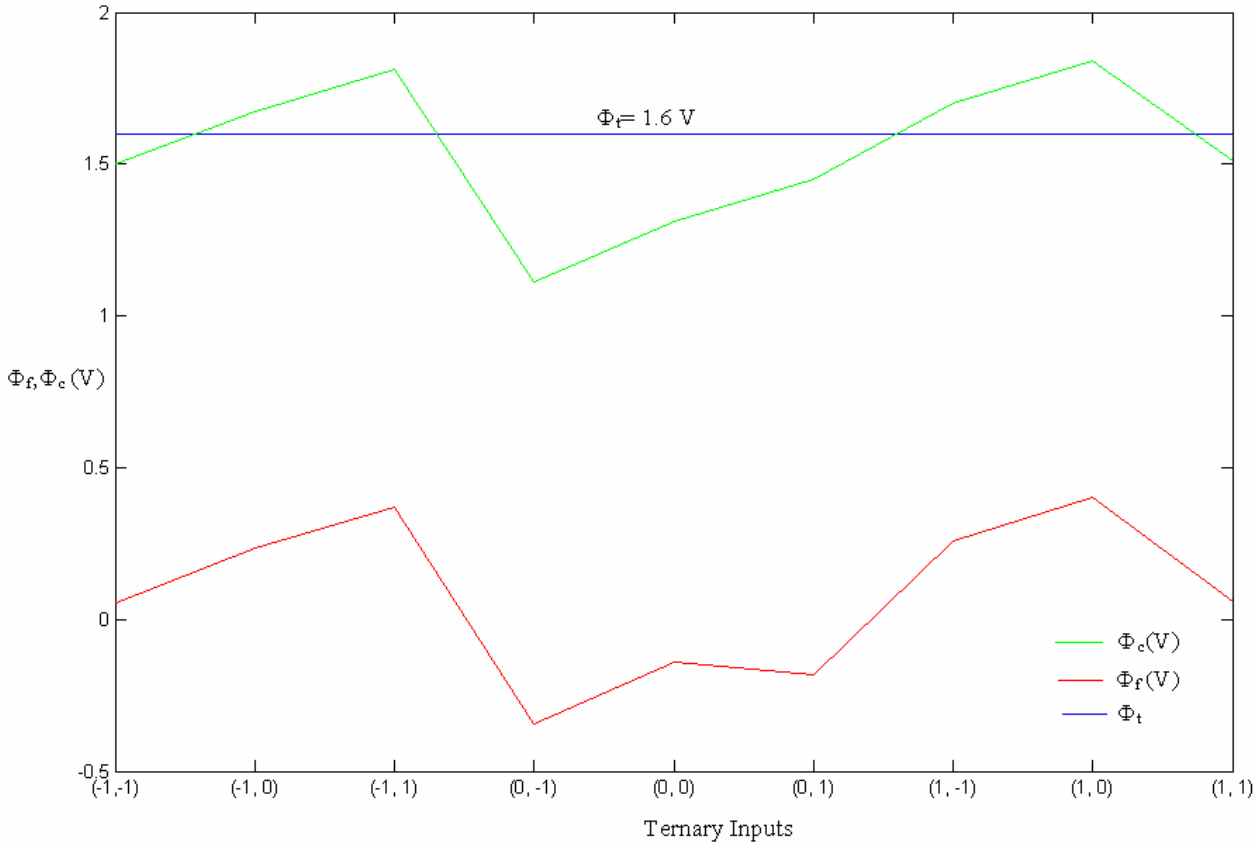


Figure 3.10. FPD of the SSB Circuit of Figure 3.8 (Stage #6).

Note: x = 1.45V

Table 3.5. Gate Voltages for Ternary Inputs of SSB Main Inverter Stage #6 With and Without Bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.6V)	Binary Output	Expected Output	SSB*	Φ_c (V) x_6 = 1.45V	Φ_f vs. Φ_t (Φ_t=1.6V)
(-1, -1)	0.054	$\Phi_f < \Phi_t$	1	1	0	1.5	$\Phi_c < \Phi_t$
(-1, 0)	0.235	$\Phi_f < \Phi_t$	1	0	1	1.674	$\Phi_c > \Phi_t$
(-1, 1)	0.37	$\Phi_f < \Phi_t$	1	0	1	1.81	$\Phi_c > \Phi_t$
(0, -1)	-0.344	$\Phi_f < \Phi_t$	1	1	0	1.11	$\Phi_c < \Phi_t$
(0, 0)	-0.142	$\Phi_f < \Phi_t$	1	1	0	1.31	$\Phi_c < \Phi_t$
(0, 1)	-0.183	$\Phi_f < \Phi_t$	1	1	0	1.451	$\Phi_c < \Phi_t$
(1, -1)	0.259	$\Phi_f < \Phi_t$	1	0	1	1.7	$\Phi_c > \Phi_t$
(1, 0)	0.401	$\Phi_f < \Phi_t$	1	0	1	1.84	$\Phi_c > \Phi_t$
(1, 1)	0.06	$\Phi_f < \Phi_t$	1	1	0	1.51	$\Phi_c < \Phi_t$

* SSB is obtained by complementing the expected output by using an inverter.

The biasing technique as described in earlier section is again employed to determine the modulated gate voltage after biasing the floating gate potential Φ_f to obtain the correct output. The FPD for stage #4 showing the floating gate potential after biasing, Φ_c for different ternary inputs is also shown in Figure 3.11. The computed value of x_4 is 1.25 V. The values of Φ_f and Φ_c are shown in Table 3.6 and compared with Φ_t to obtain the correct output.

3.4.2 Circuit Design for Pre-input Gate Inverter Stage #5 for SSB

The output of stage #5, V_5, goes LOW (0 V) from inputs $(0, -1)_3$ to $(1, 1)_3$ [8]. This stage requires three input capacitors C_9, C_{10} and C_{11} which have inputs V_A, V_B and V_{DD}, respectively. The threshold voltage, Φ_t, can be calculated from Figure 3.9 and is 1.48 V for a W/L of 41.7 μm / 2.1 μm for p-MOS and 6.6 μm / 2.1 μm for the n-MOS transistor. Using design equations (3.12) to (3.14) the values of C_9, C_{10} and C_{11} are found to be 1250 fF, 250 fF and 1000 fF, respectively. The FPD for the stage #5 showing Φ_f for different inputs is shown in Figure 3.12. The biasing technique as described in earlier section is again employed to determine the modulated gate voltage after biasing the floating gate potential Φ_t to obtain the correct output. The FPD stage #5 showing the potential after biasing, Φ_c, for different ternary inputs is also shown in Figure 3.12. The computed value of x_5 is 2.55V. The values of Φ_f and Φ_c are given in Table 3.7 and compared with Φ_t to obtain the correct output.

3.5 Circuit Design for Least Significant Bit (LSB)

The output of the LSB is LOW (0 V) for even decimal numbers (-4, -2, 0, 2, 4) and is logic HIGH (3 V) for the rest of the inputs (-3, -1, 1, 3). Figure 3.13 shows the LSB circuit diagram. In the design of the LSB, the threshold voltage Φ_t of stage #11 is

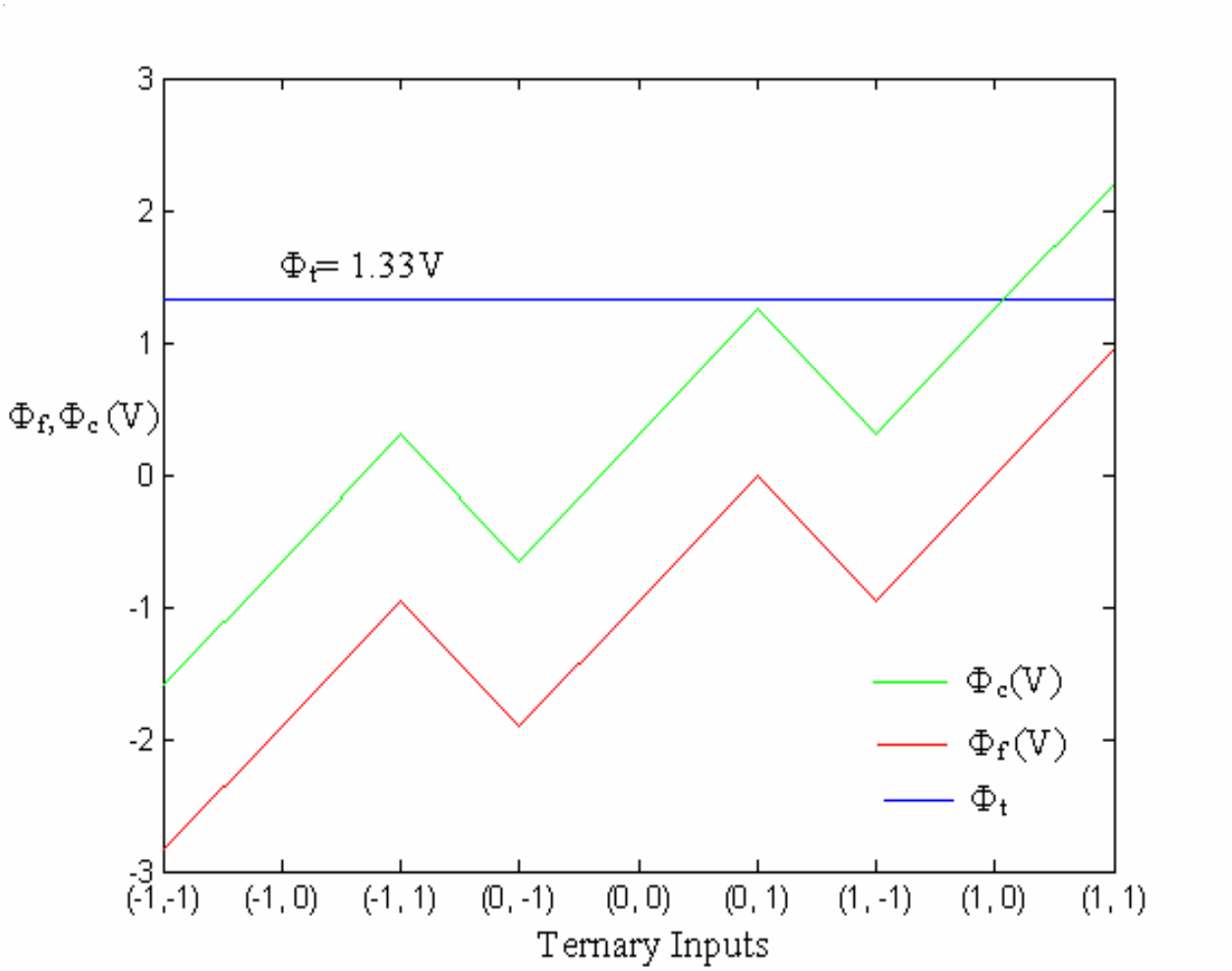


Figure 3.11. FPD of the SSB Circuit of Figure 3.8 (Stage #4).

Note: $x_4 = 1.25V$

Table 3.6. Gate Voltages for Ternary Inputs of SSB Stage #4 With and Without Bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.323V)	Binary Output	Expected Output	Φ_c (V) x_4 = 1.25V	Φ_c vs. Φ_t (Φ_t=1.323V)
(-1, -1)	-1.55	$\Phi_f < \Phi_t$	1	1	0.993	$\Phi_c < \Phi_t$
(-1, 0)	-1.33	$\Phi_f < \Phi_t$	1	1	1.2121	$\Phi_c < \Phi_t$
(-1, 1)	-1.11	$\Phi_f < \Phi_t$	1	1	1.43	$\Phi_c < \Phi_t$
(0, -1)	-0.443	$\Phi_f < \Phi_t$	1	0	2.094	$\Phi_c > \Phi_t$
(0, 0)	-0.222	$\Phi_f < \Phi_t$	1	0	2.32	$\Phi_c > \Phi_t$
(0, 1)	0.004	$\Phi_f < \Phi_t$	1	0	2.55	$\Phi_c > \Phi_t$
(1, -1)	0.665	$\Phi_f < \Phi_t$	1	0	3.23	$\Phi_c > \Phi_t$
(1, 0)	0.885	$\Phi_f < \Phi_t$	1	0	3.46	$\Phi_c > \Phi_t$
(1, 1)	1.105	$\Phi_f < \Phi_t$	1	0	3.68	$\Phi_c > \Phi_t$

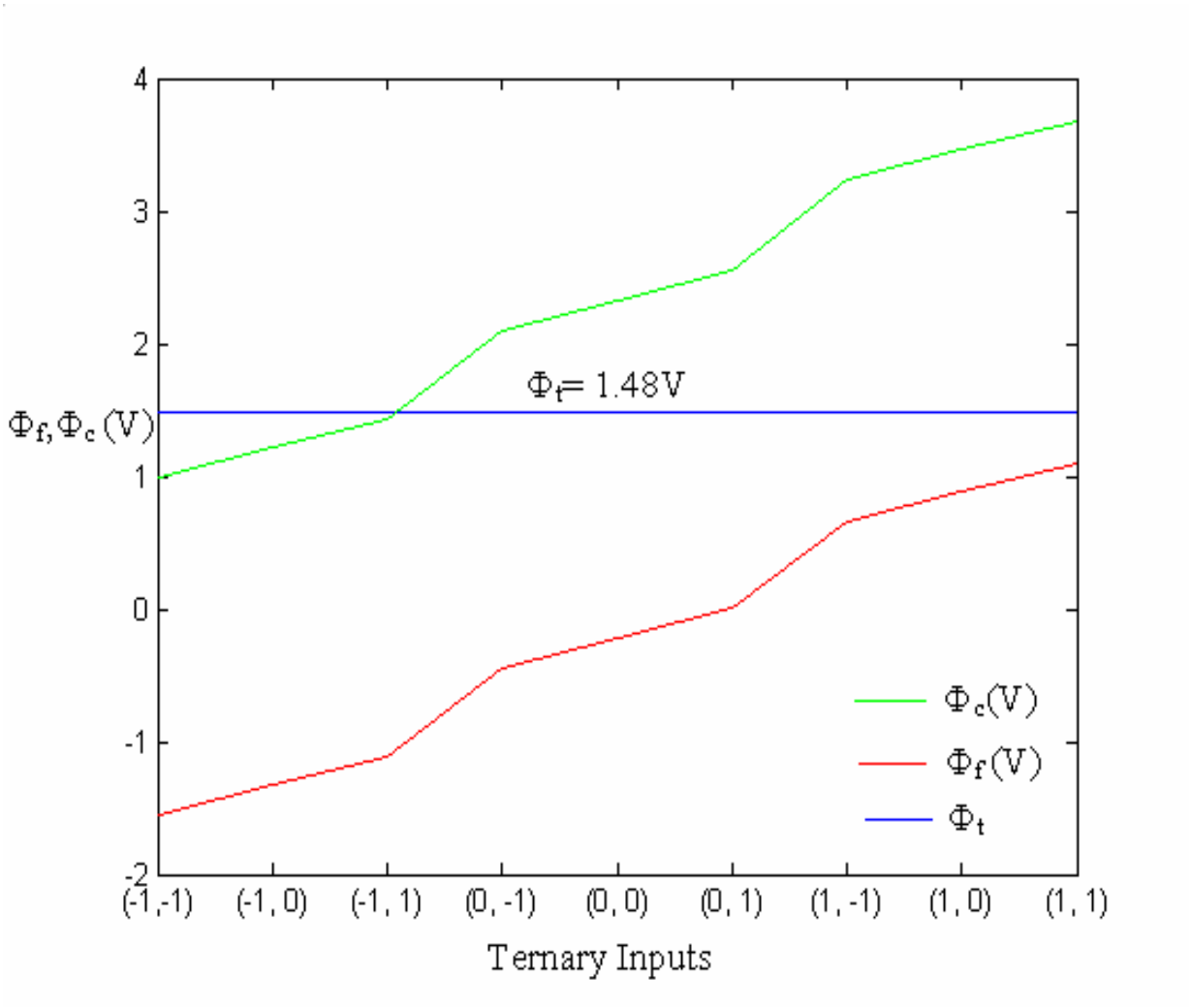


Figure 3.12. FPD of the SSB Circuit of Figure 3.8 (Stage #5).

Note: x = 1.48V

Table 3.7. Gate Voltages for Ternary Inputs of SSB Stage #5 With and Without Bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.48V)	Binary Output	Expected Output	Φ_c (V) x_5 = 2.55V	Φ_c vs. Φ_t (Φ_t=1.48V)
(-1, -1)	-2.84	$\Phi_f < \Phi_t$	1	1	-1.59	$\Phi_c < \Phi_t$
(-1, 0)	-1.9	$\Phi_f < \Phi_t$	1	1	-0.653	$\Phi_c < \Phi_t$
(-1, 1)	-0.963	$\Phi_f < \Phi_t$	1	1	0.315	$\Phi_c < \Phi_t$
(0, -1)	-1.91	$\Phi_f < \Phi_t$	1	1	-0.655	$\Phi_c < \Phi_t$
(0, 0)	-0.963	$\Phi_f < \Phi_t$	1	1	0.315	$\Phi_c < \Phi_t$
(0, 1)	-0.001	$\Phi_f < \Phi_t$	1	1	1.25	$\Phi_c < \Phi_t$
(1, -1)	-0.963	$\Phi_f < \Phi_t$	1	1	0.315	$\Phi_c < \Phi_t$
(1, 0)	-0.0023	$\Phi_f < \Phi_t$	1	1	1.25	$\Phi_c < \Phi_t$
(1, 1)	0.959	$\Phi_f < \Phi_t$	1	0	2.2	$\Phi_c > \Phi_t$

calculated and compared with Φ_t. It is observed from Table 3.1 that Φ_f falls below the switching threshold voltage four times and hence we need four pre-input gate inverter stages to design the LSB. The inverter stage #11 has six input capacitors (C_{21}, C_{22}, C_{23},

C_{24}, C_{25} and C_{26}). Inputs V_A and V_B control capacitors C_{21} and C_{22}, respectively. C_{23}, C_{24}, C_{25} and C_{26} are controlled by outputs of the pre-inverter stages V_7 (stage #7), V_8 (stage #80, V_9 (stage #9) and V_{10} (stage #10), respectively. The output V_7 (stage #7) goes LOW (0 V) from inputs $(-1, 1)_3$ to $(1, 1)_3$ and the output V_8 (stage #8) goes LOW (0 V) from inputs $(0, 0)_3$ to $(1, 1)_3$ [8]. The output V_9 (stage #9) goes LOW (0 V) from $(1, -1)_3$ to $(1, 1)_3$ and output V_{10} goes LOW (0 V) for input $(1, 1)_3$.

Design equations for stage #11 are as follows [8].

$$\phi_F = \frac{V_A C_{21} + V_B C_{22} + V_7 C_{23} + V_8 C_{24} + V_9 C_{25} + V_{10} C_{26} + V_{DD} C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxp} + C_p + C_{oxn}}. \tag{3.15}$$

For inputs $(-1, -1)_3$,

$$\phi_F = \frac{(-3V) C_{21} + (-3V) C_{22} + V_7 C_{23} + V_8 C_{24} + V_9 C_{25} + V_{10} C_{26} + V_{DD} C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxp} + C_p + C_{oxn}} < \phi_t . \tag{3.16}$$

For input $(-1, 0)_3$,

$$\phi_F = \frac{(-3V) C_{21} + (0V) C_{22} + V_7 C_{23} + V_8 C_{24} + V_9 C_{25} + V_{10} C_{26} + V_{DD} C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxp} + C_p + C_{oxn}} > \phi_t . \tag{3.17}$$

For input $(-1, 1)_3$,

$$\phi_F = \frac{(-3V) C_{21} + (3V) C_{22} + V_7 C_{23} + V_8 C_{24} + V_9 C_{25} + V_{10} C_{26} + V_{DD} C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxp} + C_p + C_{oxn}} < \phi_t . \tag{3.18}$$

Figure 3.14 shows the VTC of all inverter stages shown in Figure 3.13. The value of Φ_t can be calculated from Figure 3.14 by taking the average of Φ_{g0} and Φ_{s1} which are obtained for a W/L of 13.8 µm / 2.1 µm for pMOS and 5.7 µm / 2.1 µm for nMOS transistors. Substituting Φ_t in equations 3.15-3.18, C_{21}, C_{22}, C_{23}, $C_{24,}$ C_{25} and C_{26} are

found to be 500 fF, 250 fF, 500 fF, 500 fF, 250 fF and 500 fF, respectively. The FPD for stage #11 of the LSB is plotted in Figure 3.15.

The biasing technique as described in earlier section is employed to determine the modulated gate voltage after biasing the floating gate potential Φ_f to obtain the correct output. The FPD for stage #11 showing the floating gate potential after biasing Φ_c for different ternary inputs is also shown in Figure 3.15. The computed value of x_{11} is 1.39 V. The values of Φ_f and Φ_c are given in Table 3.8 and compared with Φ_t to obtain the correct output. Φ_t was found to be 1.3016 V for this stage. The output of the inverter stage #11 is passed though another inverter to obtain the LSB. Hence in Table 3.8, the expected output is the complement of the LSB.

3.5.1 Circuit Design for Pre-input Gate Inverter Stage #7 for LSB

The output of stage #7, V_7, goes LOW (0 V) from inputs $(-1, 1)_3$ to $(1, 1)_3$. This stage requires two input capacitors C_{16} and C_{17} which have inputs V_A and V_B respectively. The threshold voltage, Φ_t can be calculated from Figure 3.14 and is equal to Φ_t=1.2718 V for a W/L of 30.15 μm / 2.1 μm for the p-MOS and 13.2 μm / 2.1 μm for the n-MOS transistors, respectively. From equations (3.15) to (3.18) the values of C_{16} and C_{17} are set at 750 fF and 250 fF, respectively. The FPD for the stage #7 showing Φ_f for different inputs is shown in Figure 3.16. The biasing technique as described in earlier section is again employed to determine the modulated gate voltage after biasing the floating gate potential Φ_f to obtain the correct output. The FPD for stage #7 showing the floating gate potential after biasing, Φ_c for different ternary inputs is also shown in Figure 3.16. The computed value of x_7 is 2.28 V. The values of Φ_f and Φ_c are compared in Table 3.9, with Φ_t, to obtain the correct output.

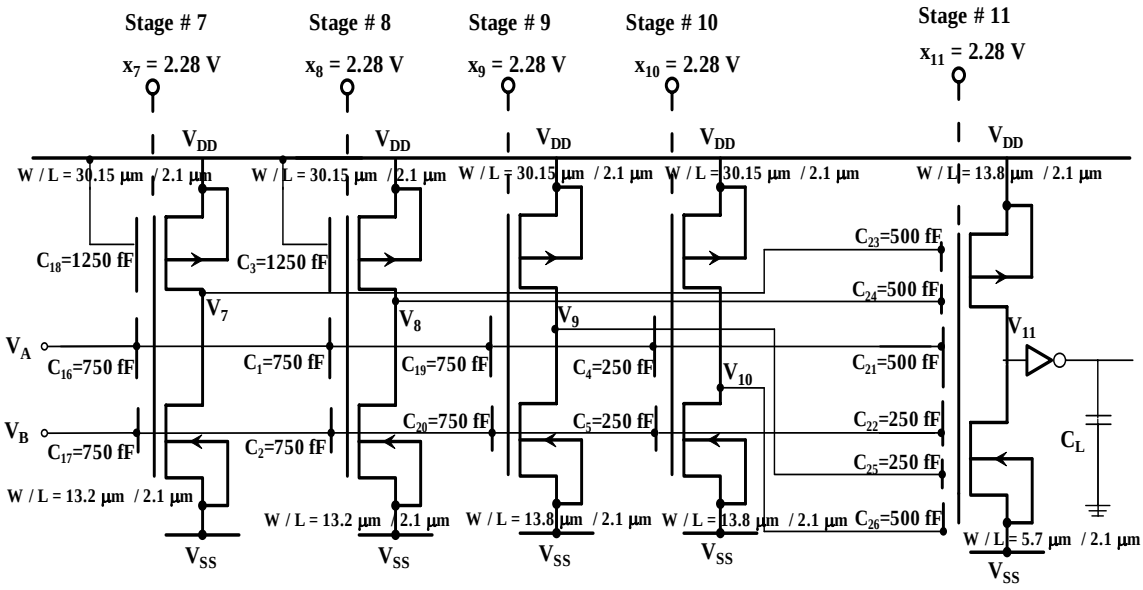


Figure 3.13. LSB Circuit Diagram.

Note: V_{DD} = 3 V and V_{SS} = 0 V.

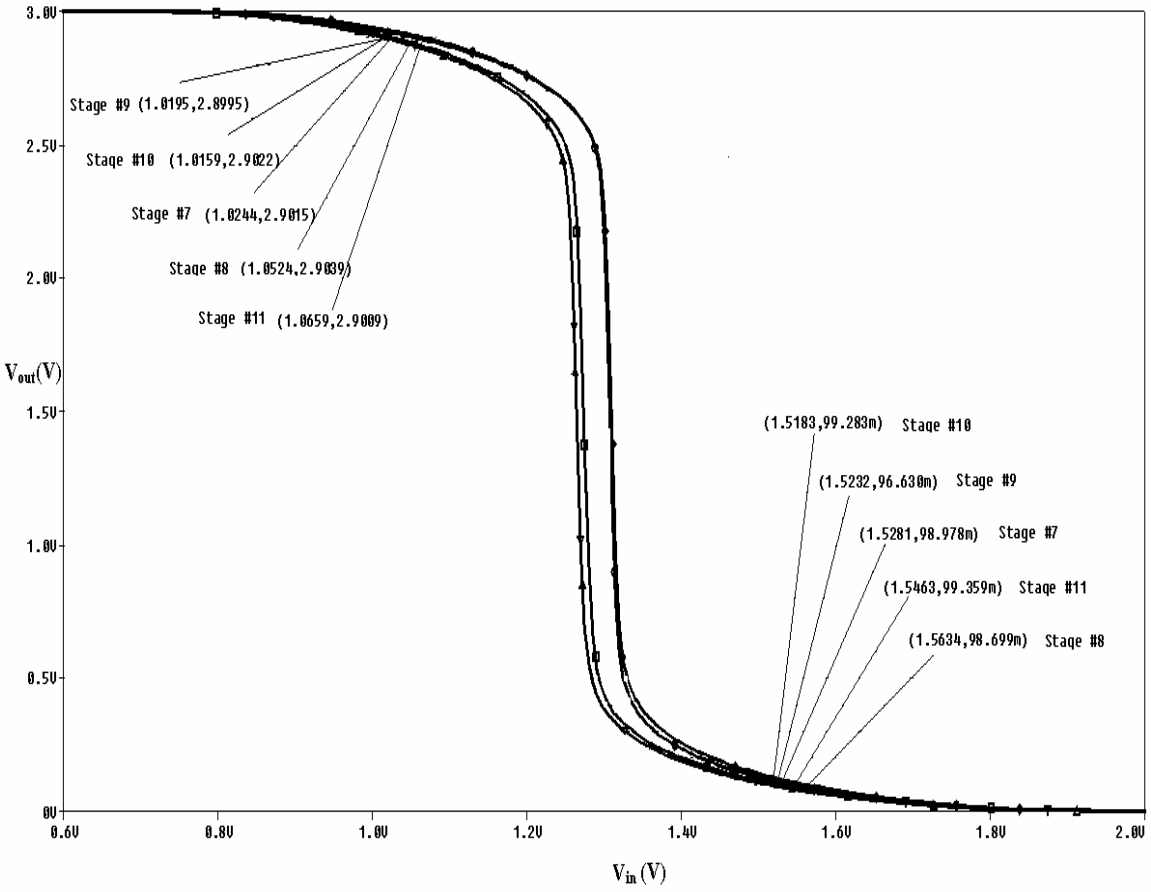


Figure 3.14. VTC of the LSB Circuit Diagram of Figure 3.13.

Note: The x coordinates of the points in the upper half of the curves represent the Φ_{g0} and the x coordinates of the points in the lower half represent Φ_{s1} of the respective curves for the five stages of the LSB.

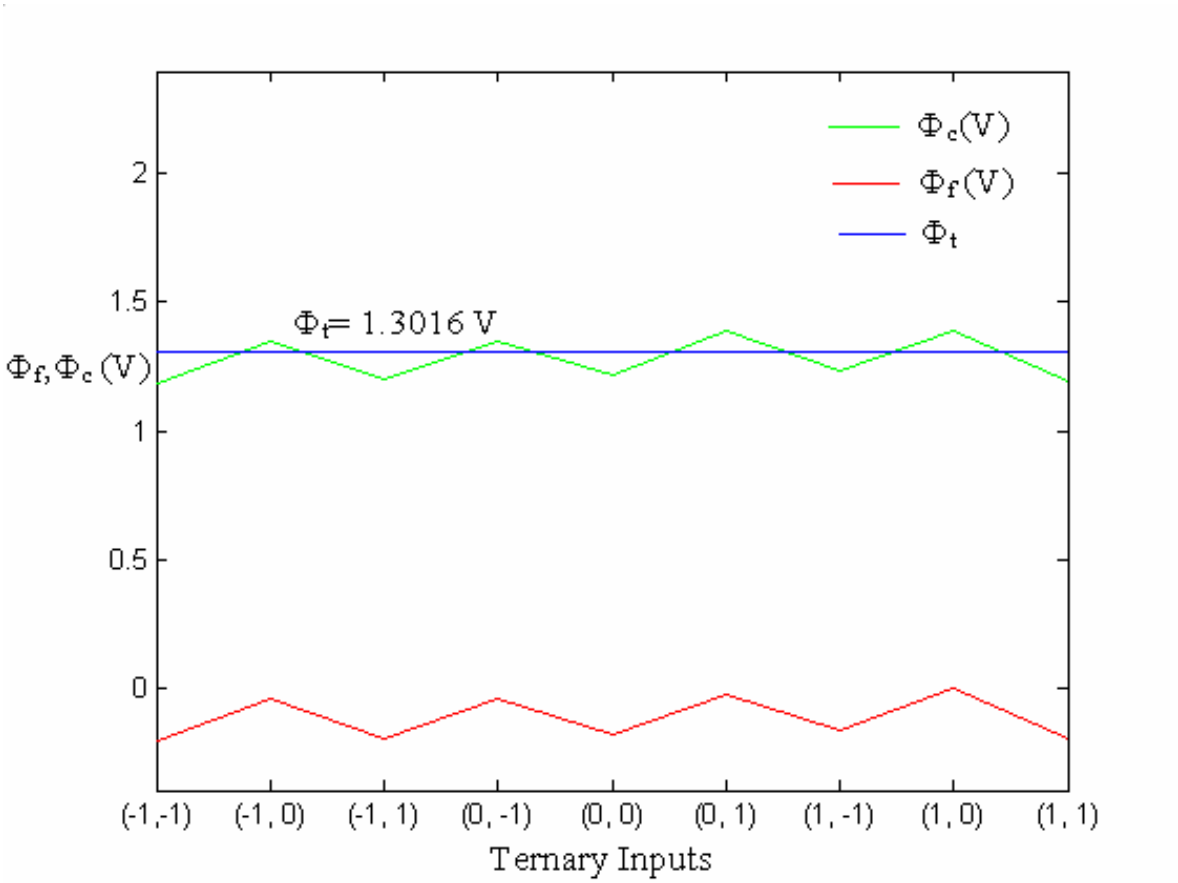


Figure 3.15. FPD for LSB (Stage #11) of Figure 3.13.

Note: x_{11} = 1.39V.

Table 3.8. Gate voltages for ternary inputs of LSB stage #11 with and without bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.3016V)	Binary Output	Expected Output	* LSB	Φ_c (V) x_{11} = .39V	Φ_c vs. Φ_t (Φ_t=1.3016 V)
(-1, -1)	-0.2111	$\Phi_f < \Phi_t$	1	1	0	1.184	$\Phi_c < \Phi_t$
(-1, 0)	-0.0407	$\Phi_f < \Phi_t$	1	0	1	1.3499	$\Phi_c > \Phi_t$
(-1, 1)	-0.1959	$\Phi_f < \Phi_t$	1	1	0	1.1993	$\Phi_c < \Phi_t$
(0, -1)	-0.0411	$\Phi_f < \Phi_t$	1	0	1	1.3486	$\Phi_c > \Phi_t$
(0, 0)	-0.1829	$\Phi_f < \Phi_t$	1	1	0	1.2093	$\Phi_c < \Phi_t$
(0, 1)	-0.0303	$\Phi_f < \Phi_t$	1	0	1	1.3901	$\Phi_c > \Phi_t$
(1, -1)	-0.1688	$\Phi_f < \Phi_t$	1	1	0	1.2301	$\Phi_c < \Phi_t$
(1, 0)	-0.0009	$\Phi_f < \Phi_t$	1	0	1	1.3892	$\Phi_c > \Phi_t$
(1, 1)	-0.2021	$\Phi_f < \Phi_t$	1	1	0	1.1927	$\Phi_c < \Phi_t$

* LSB is obtained by complementing the expected output by using an inverter.

3.5.2 Circuit Design for Pre-input Gate Inverter Stage #8 for LSB

The output of stage #8, V_8 goes LOW (0 V) from inputs $(0, 0)_3$ to $(1, 1)_3$ [8]. It is noticed here that the output of this stage is same as that of the sign bit. This stage requires two input capacitors C_1 and C_2 which have inputs V_A and V_B, respectively. The sizes of the capacitors are set in the ratio 3:1 according to the weights of MSB and LSB in ternary bits. The threshold voltage can be calculated from Figure 3.14 and is equal to 1.3129 V for a W/L of 30.15 µm / 2.1 µm for p-MOS and 11.1 µm / 2.1 µm for the n-MOS transistors. The value of C_1 and C_2 are set at 750 fF and 250 fF, respectively. A third capacitor C_3 is required so that equations (3.15) to (3.18) are satisfied. The FPD for stage #8 showing Φ_f for different inputs is shown in Figure 3.17. The FPD for the stage #8 showing the floating gate potential after biasing, Φ_c for different ternary inputs is also shown in Figure 3.17. The computed value of x_8 is 1.75 V. The values of Φ_f and Φ_c are given in Table 3.10 and compared with Φ_t to obtain the correct output.

3.5.3 Circuit Design for Pre-input Gate Inverter Stage #9 for LSB

The output of stage #9, V_9 goes LOW (0 V) from inputs $(1, -1)_3$ to $(1, 1)_3$. This stage requires two input capacitors C_{19} and C_{20}, which have inputs V_A and V_B, respectively. The threshold voltage Φ_t can be calculated from Figure 3.14 and is 1.267 V

for a W/L of 30.15 µm / 2.1 µm for p-MOS and 13.8 µm / 2.1 µm for the n-MOS transistors, respectively. The values of C_{19} and C_{20} are set at 750 fF and 250 fF respectively so that equations (3.15) to (3.18) are satisfied. The FPD for stage #9 showing Φ_f for different inputs is shown in Figure 3.18. The FPD for stage #9 showing the

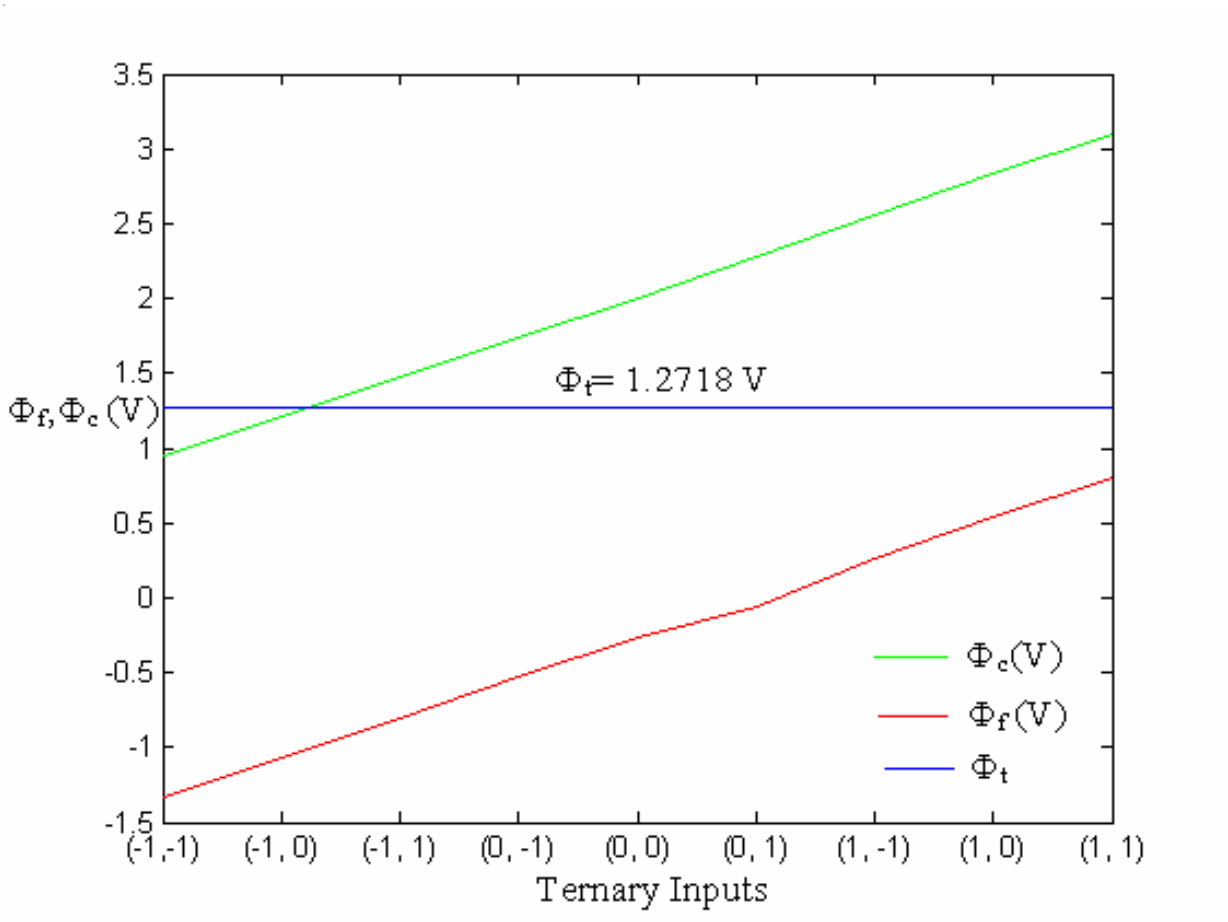


Figure 3.16. FPD for LSB (Stage #7) of Figure 3.13.

Note x_7 = 2.28 V.

Table 3.9. Gate Voltages for Ternary Inputs of LSB Stage #7 With and Without Bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.2718V)	Binary Output	Expected Output	Φ_c (V) x_7 = 2.28V	Φ_c vs. Φ_t (Φ_t=1.2718V)
(-1, -1)	-1.332	$\Phi_f < \Phi_t$	1	1	0.7	$\Phi_c < \Phi_t$
(-1, 0)	-1.07	$\Phi_f < \Phi_t$	1	1	1.22	$\Phi_c < \Phi_t$
(-1, 1)	-0.802	$\Phi_f < \Phi_t$	1	0	1.47	$\Phi_c > \Phi_t$
(0, -1)	-0.535	$\Phi_f < \Phi_t$	1	0	1.74	$\Phi_c > \Phi_t$
(0, 0)	-0.267	$\Phi_f < \Phi_t$	1	0	2.01	$\Phi_c > \Phi_t$
(0, 1)	-0.066	$\Phi_f < \Phi_t$	1	0	2.28	$\Phi_c > \Phi_t$
(1, -1)	0.268	$\Phi_f < \Phi_t$	1	0	2.555	$\Phi_c > \Phi_t$
(1, 0)	0.536	$\Phi_f < \Phi_t$	1	0	2.828	$\Phi_c > \Phi_t$
(1, 1)	0.803	$\Phi_f < \Phi_t$	1	0	3.1001	$\Phi_c > \Phi_t$

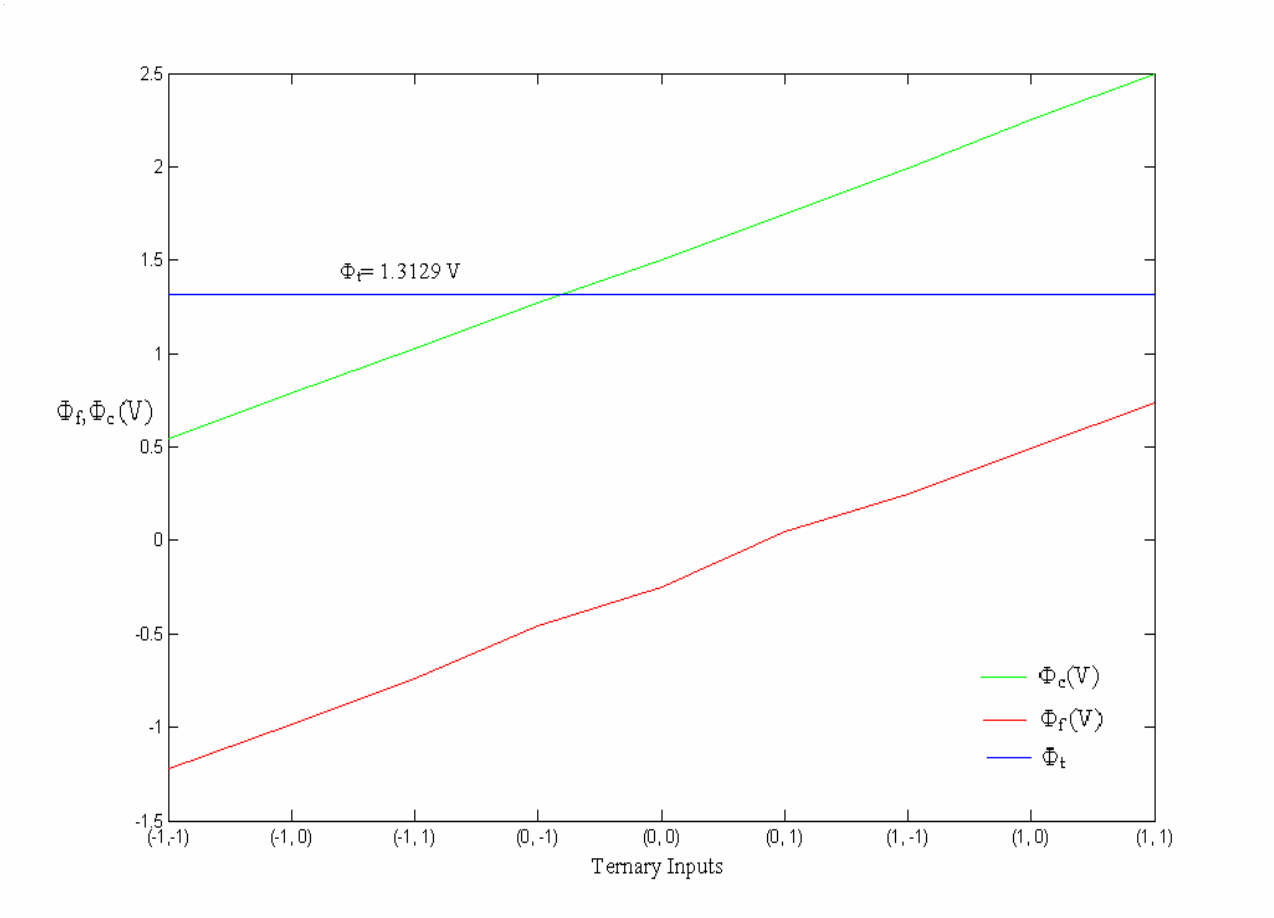


Figure 3.17. FPD for LSB (Stage #8) of Figure 3.13.

Note x_8 = 1.75 V.

Table 3.10. Gate Voltages for Ternary Inputs of LSB Stage #8 With and Without Bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.3129V)	Binary Output	Expected Output	Φ_c (V) x_8 = 0.85V	Φ_c vs. Φ_t (Φ_t=1.3129V)
(-1, -1)	-1.223	$\Phi_f < \Phi_t$	1	1	0.541	$\Phi_c < \Phi_t$
(-1, 0)	-0.982	$\Phi_f < \Phi_t$	1	1	0.786	$\Phi_c < \Phi_t$
(-1, 1)	-0.738	$\Phi_f < \Phi_t$	1	1	1.029	$\Phi_c < \Phi_t$
(0, -1)	-0.459	$\Phi_f < \Phi_t$	1	1	1.27	$\Phi_c < \Phi_t$
(0, 0)	-0.246	$\Phi_f < \Phi_t$	1	0	1.5	$\Phi_c > \Phi_t$
(0, 1)	0.046	$\Phi_f < \Phi_t$	1	0	1.75	$\Phi_c > \Phi_t$
(1, -1)	0.246	$\Phi_f < \Phi_t$	1	0	1.99	$\Phi_c > \Phi_t$
(1, 0)	0.493	$\Phi_f < \Phi_t$	1	0	2.25	$\Phi_c > \Phi_t$
(1, 1)	0.739	$\Phi_f < \Phi_t$	1	0	2.5	$\Phi_c > \Phi_t$

floating gate potential after biasing Φ_c for different ternary inputs is also shown in Figure 3.18. The computed value of x_9 is 0.85 V. The values of Φ_f and Φ_c are given in Table 3.11 and compared with Φ_t to obtain the correct output.

3.5.4 Circuit Design for Pre-input Gate Inverter Stage #10 for LSB

The output of stage #10, V_{10} goes LOW (0 V) for input $(1, 1)_3$ [8]. The output of this gate is the same as the pre-input gate inverter stage #2 of MSB. This stage requires 2 input capacitors C_4 and C_5, which have inputs V_A and V_B respectively. The threshold voltage Φ_t can be calculated from Figure 3.14 and is 1.247 V for a W/L of 30.15 µm / 2.1 µm for p-MOS and 13.8 µm / 2.1 µm for n-MOS transistors, respectively. The values of C_4 and C_5 are set at 250 fF each so that equations (3.15) – (3.18) are satisfied. The FPD for stage #10 showing Φ_f for different inputs is shown in Figure 3.19. The FPD for stage #10 showing the floating gate potential after biasing, Φ_c, for different ternary inputs is also shown in Figure 3.19. The computed value of x_{10} is 1.0 V. The values of Φ_f and Φ_c are given in Table 3.12 and compared with Φ_t to obtain the correct output. The values of x used for each inverter stage is shown in Table 3.13.

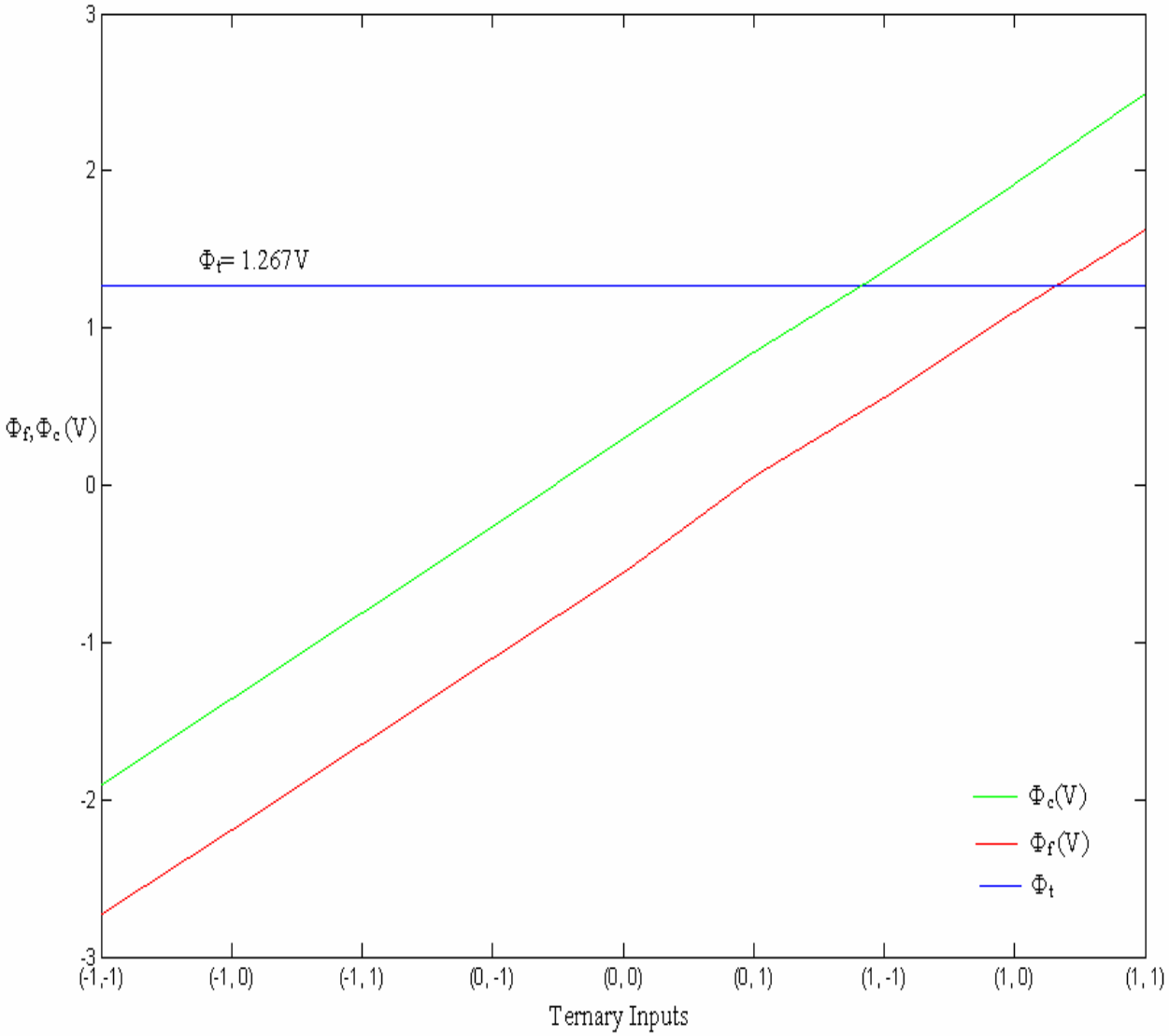


Figure 3.18. FPD for LSB (Stage #9) of Figure 3.13.

Note x_9 = 0.85 V.

Table 3.11. Gate Voltages for Ternary Inputs of LSB Stage #9 With and Without Bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.267V)	Binary Output	Expected Output	Φ_c (V) x_9 = 0.85V	Φ_c vs. Φ_t (Φ_t=1.267V)
(-1, -1)	-2.732	$\Phi_f < \Phi_t$	1	1	-1.902	$\Phi_c < \Phi_t$
(-1, 0)	-2.19	$\Phi_f < \Phi_t$	1	1	-1.36	$\Phi_c < \Phi_t$
(-1, 1)	-1.65	$\Phi_f < \Phi_t$	1	1	-0.815	$\Phi_c < \Phi_t$
(0, -1)	-1.1	$\Phi_f < \Phi_t$	1	1	-0.262	$\Phi_c < \Phi_t$
(0, 0)	-0.556	$\Phi_f < \Phi_t$	1	1	0.296	$\Phi_c < \Phi_t$
(0, 1)	0.058	$\Phi_f < \Phi_t$	1	1	0.85	$\Phi_c < \Phi_t$
(1, -1)	0.558	$\Phi_f < \Phi_t$	1	0	1.36	$\Phi_c > \Phi_t$
(1, 0)	1.099	$\Phi_f < \Phi_t$	1	0	1.91	$\Phi_c > \Phi_t$
(1, 1)	1.62	$\Phi_f > \Phi_t$	0	0	2.49	$\Phi_c > \Phi_t$

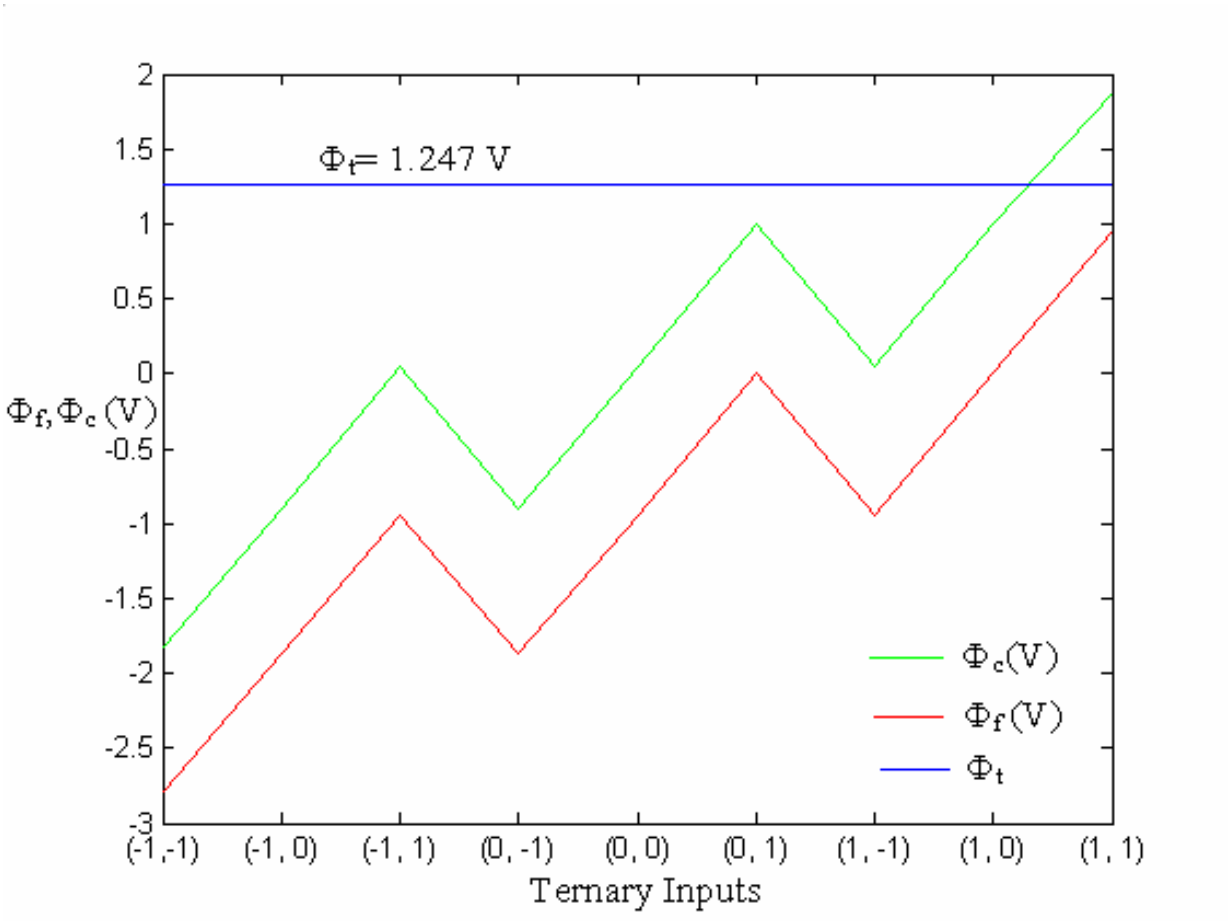


Figure 3.19. FPD for LSB (Stage #10) of Figure 3.13.

Note: x_{10} = 1.0 V.

Table 3.12. Gate Voltages for Ternary Inputs of LSB Stage #10 With and Without bias

Ternary Inputs	Φ_f (V)	Φ_f vs. Φ_t (Φ_t=1.247V)	Binary Output	Expected Output	Φ_c (V) x_{10} = 1.0V	Φ_c vs. Φ_t (Φ_t=1.247V)
(-1, -1)	-2.794	$\Phi_f < \Phi_t$	1	1	-1.82	$\Phi_c < \Phi_t$
(-1, 0)	-1.874	$\Phi_f < \Phi_t$	1	1	-0.901	$\Phi_c < \Phi_t$
(-1, 1)	-0.2	$\Phi_f < \Phi_t$	1	1	0.05	$\Phi_c < \Phi_t$
(0, -1)	-1.874	$\Phi_f < \Phi_t$	1	1	-0.902	$\Phi_c < \Phi_t$
(0, 0)	-0.3	$\Phi_f < \Phi_t$	1	1	0.052	$\Phi_c < \Phi_t$
(0, 1)	-0.001	$\Phi_f < \Phi_t$	1	1	0.999	$\Phi_c < \Phi_t$
(1, -1)	-0.3	$\Phi_f < \Phi_t$	1	1	0.051	$\Phi_c < \Phi_t$
(1, 0)	-0.0017	$\Phi_f < \Phi_t$	1	1	0.999	$\Phi_c < \Phi_t$
(1, 1)	0.949	$\Phi_f < \Phi_t$	1	0	1.8777	$\Phi_c > \Phi_t$

Table 3.13. Various Values of x Used for all the Stages

Bit	SB	MSB		SSB			LSB				
Stage number	1	2	3	4	5	6	7	8	9	10	11
x_i (V)	1.0	1.45	1.45	1.25	2.25	1.45	2.28	1.75	0.85	1.0	1.39

Chapter 4. Physical Design

4.1 Design of a Unit Capacitance

In analog integrated circuits, capacitors are designed as integer multiples of a small unit size capacitance. The concept maintains the ratio accuracy. The choice of square shape of the capacitor provides the smallest perimeter area ratio which minimizes the effect of random fluctuations. The minimum allowable value of the unit capacitor is decided based on technological considerations so that it will provide an acceptable accuracy ratio for the intended application. In the present work, the unit size capacitance is 250 fF in 0.5 μm n-well CMOS process. Figure 4.1 shows the layout of a 250 fF unit capacitor. The layout is made symmetric in both dimensions as much as possible and is referred to as a common-centroid geometry layout in order to have better accuracy ratios [31].

4.1.1 Dummy Capacitors

In analog integrated circuit design, it is desired that all capacitors should see the same environment all around. Therefore, dummy capacitors of the same size or smaller are put across the capacitors in use. While using small size dummy capacitors it is ensured that length or width of the dummy capacitor facing the real capacitor should match.

4.1.2 Well Driven Floating Gate Transistors

A new layout structure for the floating gate MOS device on top of an isolating n-well layer was proposed in [32]. The well not only provides noise isolation for the floating device but also can be used as an additional input for threshold voltage control or

signal modulation. Figure 4.2 shows an array of capacitors of size 250 fF, 750 fF and 1250 fF laid out in centroid formation and surrounded by dummy capacitors. The unit capacitance is 250 fF and the large capacitors (750 fF and 1250 fF) are realized as integer multiples of the unit capacitance. The device is laid on an n-well for better noise isolation and to lower the parasitic capacitance between the floating gate and the substrate.

4.2 Layout for Stages of Ternary to Binary Converter

The layout for the ternary to binary bit converter is divided into four bits, the SB, MSB, SSB and LSB. The physical design of stages for each bit is described below. The layout is done using L-Edit 10.2 in 0.5 μm CMOS n-well technology. The layout has been extracted into PSPICE 15.0 and simulated using BSIM level 49 parameters obtained from MOSIS. The layout for stage #1 of the sign bit (SB) is shown in Figure 4.3 and the corresponding post-layout output simulations are shown in Figure 4.4. Figure 4.5 shows the voltage of the floating gate for the sign bit and Figure 4.6 shows the output simulations with a load of 0.1 pF. The layout for stages #2 and #3 of the most significant bit (MSB) is shown in Figure 4.7 and the corresponding post-layout output simulations are shown in Figure 4.8. Figure 4.9 shows the floating gate voltages for the most significant bit and Figure 4.10 shows the output simulations with a load of 0.1 pF. The layout for stages #4, #5 and #6 of the second significant bit (SSB) is shown in Figure 4.11. The layout for stages #4, #5 and #6 of the second significant bit (SSB) is shown in Figure 4.11 and the corresponding post-layout output simulations are shown in Figure 4.12. Figure 4.13 shows the floating gate voltages for the SSB and Figure 4.14 shows the output simulations with a load of 0.1 pF. The layout for stages #7, #8, #9, #10 and #11 of the least significant bit (LSB) is shown in Figure 4.15 and the corresponding post-layout

output simulations are shown in Figure 4.16. Figure 4.17 shows the floating gate voltages for the least significant bit and Figure 4.18 shows the output simulations with a load of 0.1 pF.

Rise time delay is taken as the amount of time it takes the output voltage to go from 10% of the Logic "1" level to 90% of the Logic "1" level.The time required for the output voltage to go from 90% of the Logic "1" level to 10% of the Logic "1" level is taken as the fall time delay. The time delays from the simulations of Figures 4.6, 4.10, 4.14, 4.18 and from the experiment for all the bits of the ternary-to-binary converter for a load of 15 pF are tabulated in Table 4.1.

The inputs V_A and V_B vary between the ranges of -3 V to 3 V. Hence the input pad for V_A and V_B need to be analog pads. Figure 4.19 shows the layout design of an analog pad. All protective circuitry was removed in order to design the analog pad. The gate input voltages were given through an analog reference pad. Figure 4.20 shows the complete layout of a ternary-to-binary bit converter in 0.5 μm n-well CMOS process. The pad pin numbers are summarized in Table 4.2 for testability analysis. Figure 4.21 shows the post-layout simulation of design shown in Figure 4.20. Figure 4.22 shows the microphotograph of the chip.

4.3 Experimental Results

The chip is tested with the value of V_{DD} set at 3.0 V and V_{SS} set at 0 V. The testing of this chip requires two arbitrary inputs varying from -3V, 0V and 3V. In order to test this chip one input was kept constant at either 3V, 0V, or -3V and the other was varied from 0V to 3V. We also need an input floating gate bias voltage which switches as the input switches. The propagation delay times are also summarized in Table 4.1 for

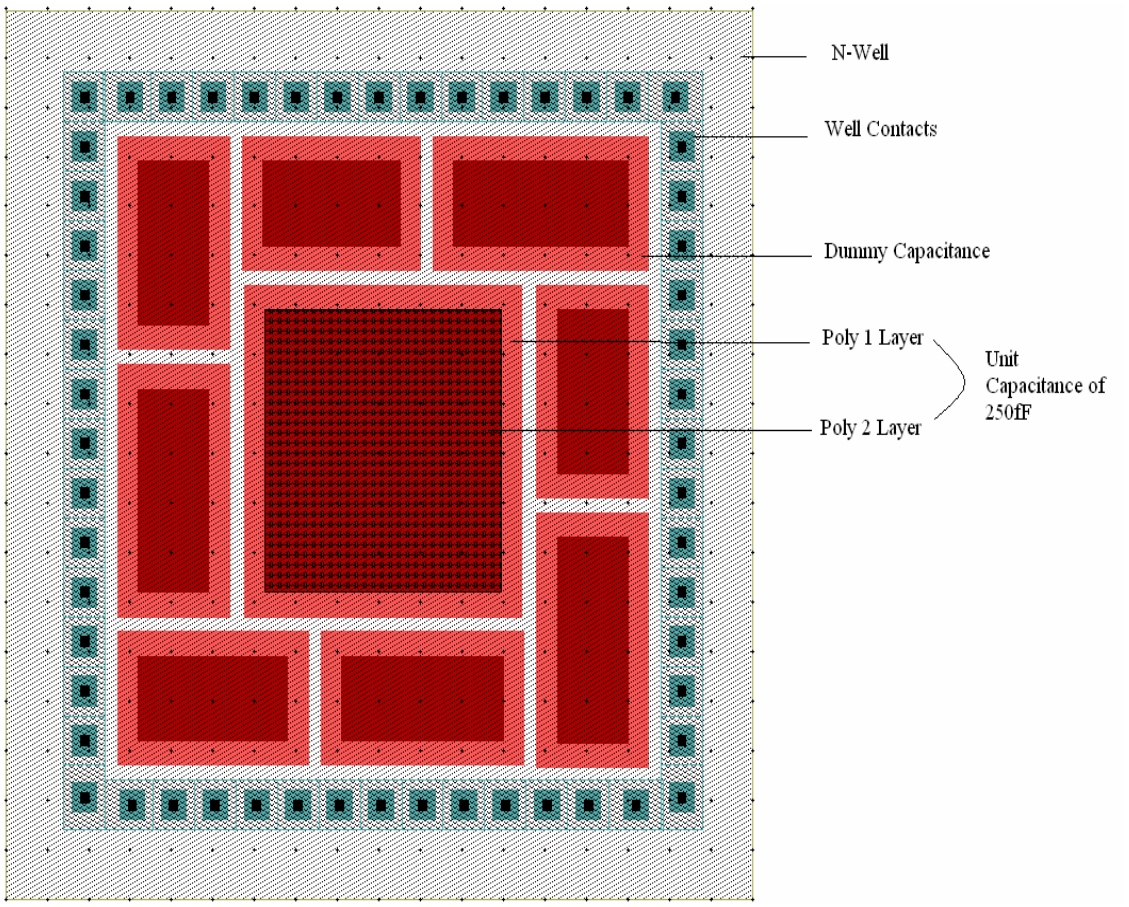


Figure 4.1. Layout of a 250 fF Unit Capacitor.

Note: The capacitor dimensions are 20.1µm x 20.1µm.

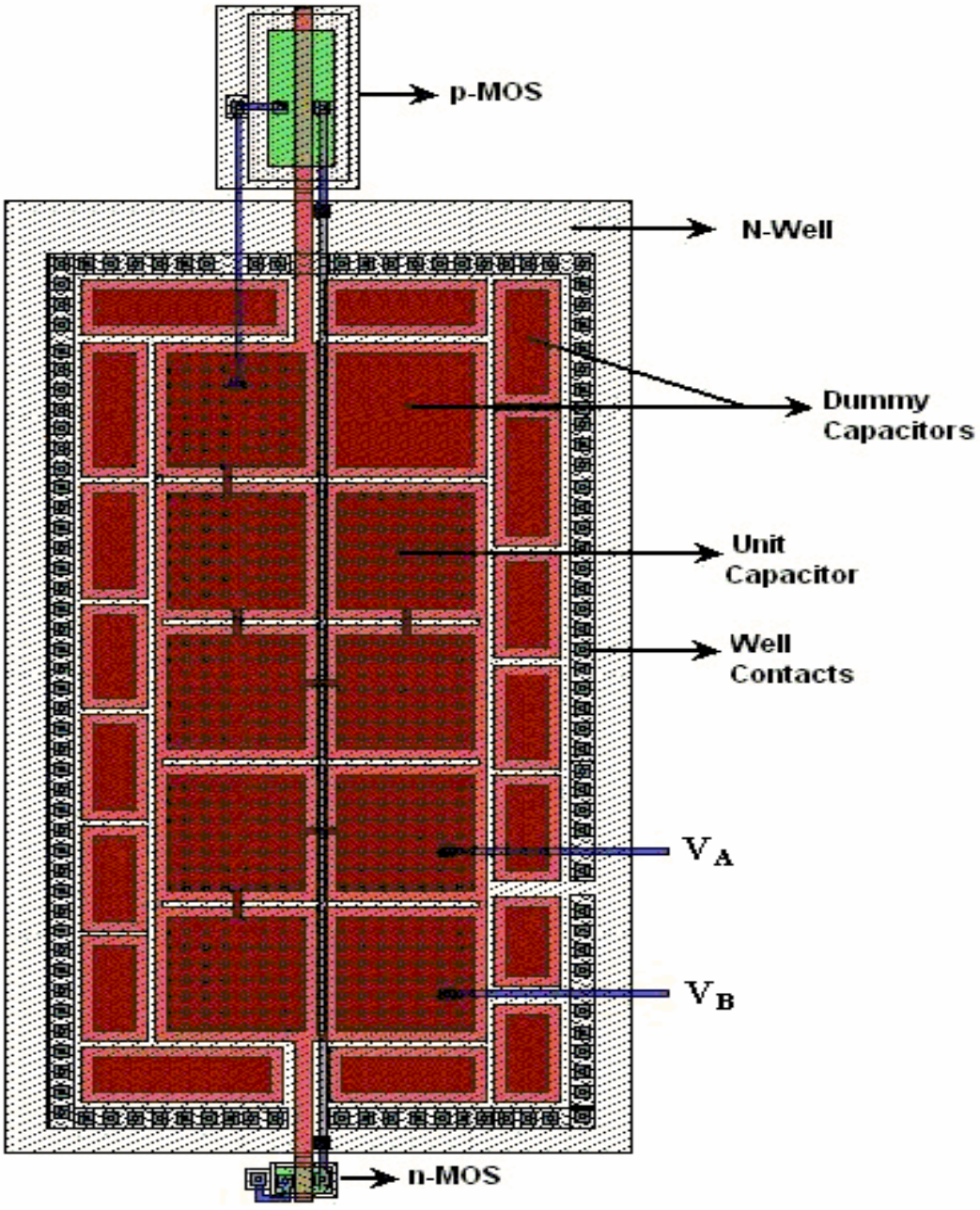


Figure 4.2. Parallel Unit Capacitors in Common-Centroid Geometry.
Note: V_A and V_B are the ternary inputs.

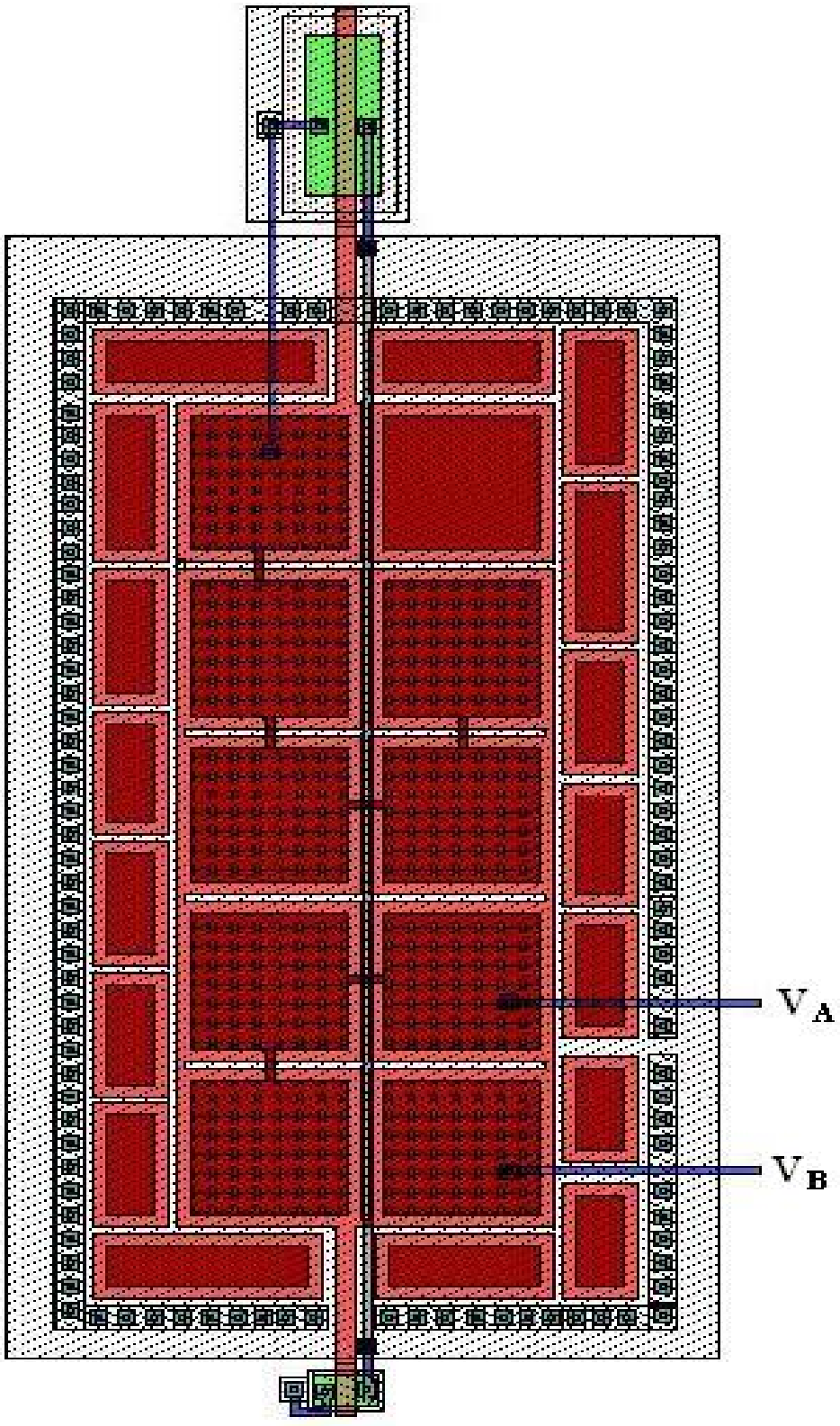


Figure 4.3. Layout for Sign Bit (SB).

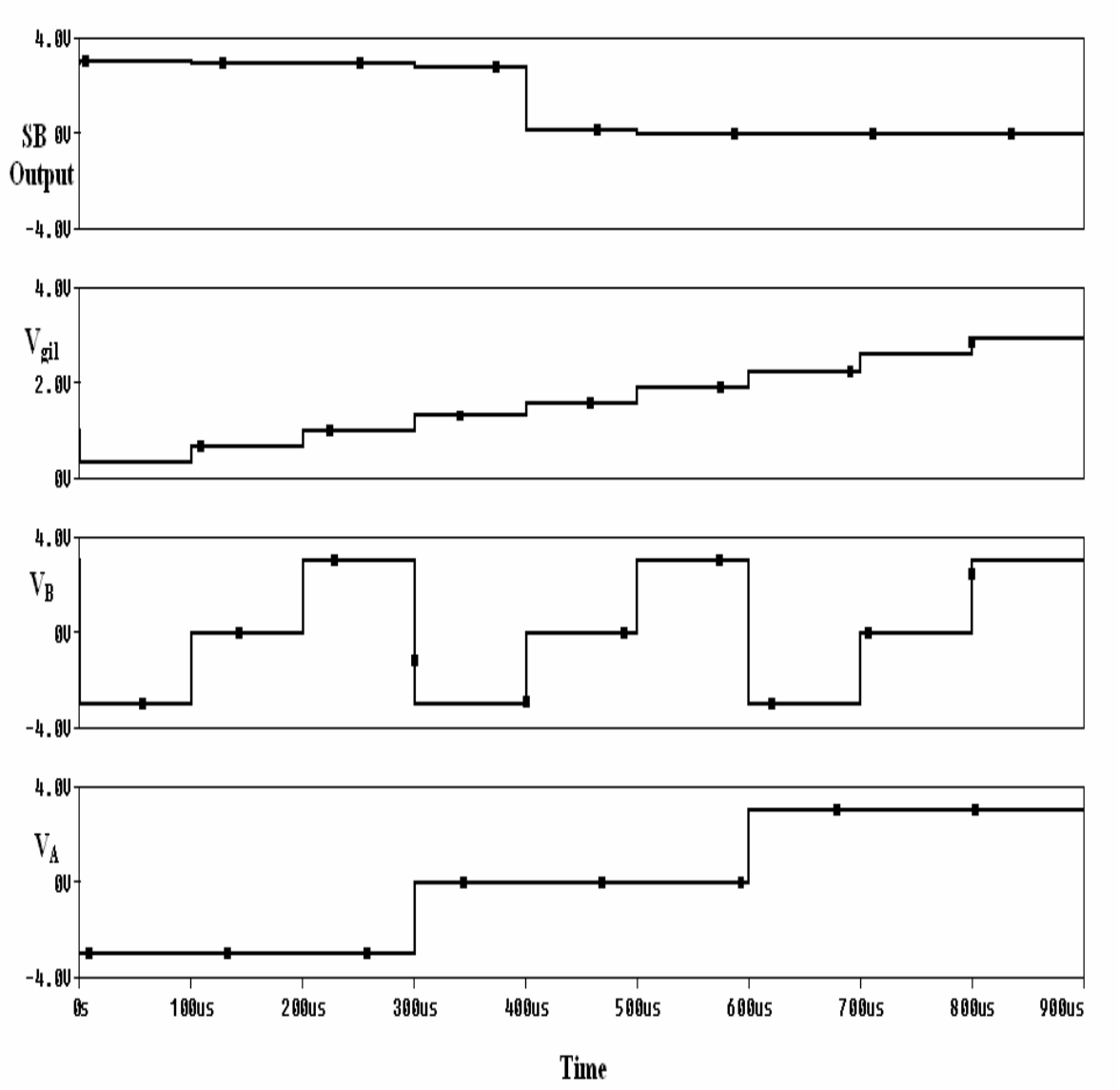


Figure 4.4. Post-Layout Simulations for Sign Bit in No Load Condition.

Note: V_A, V_B are ternary inputs and V_{gi1} is the voltage on the floating gate (stage #1).

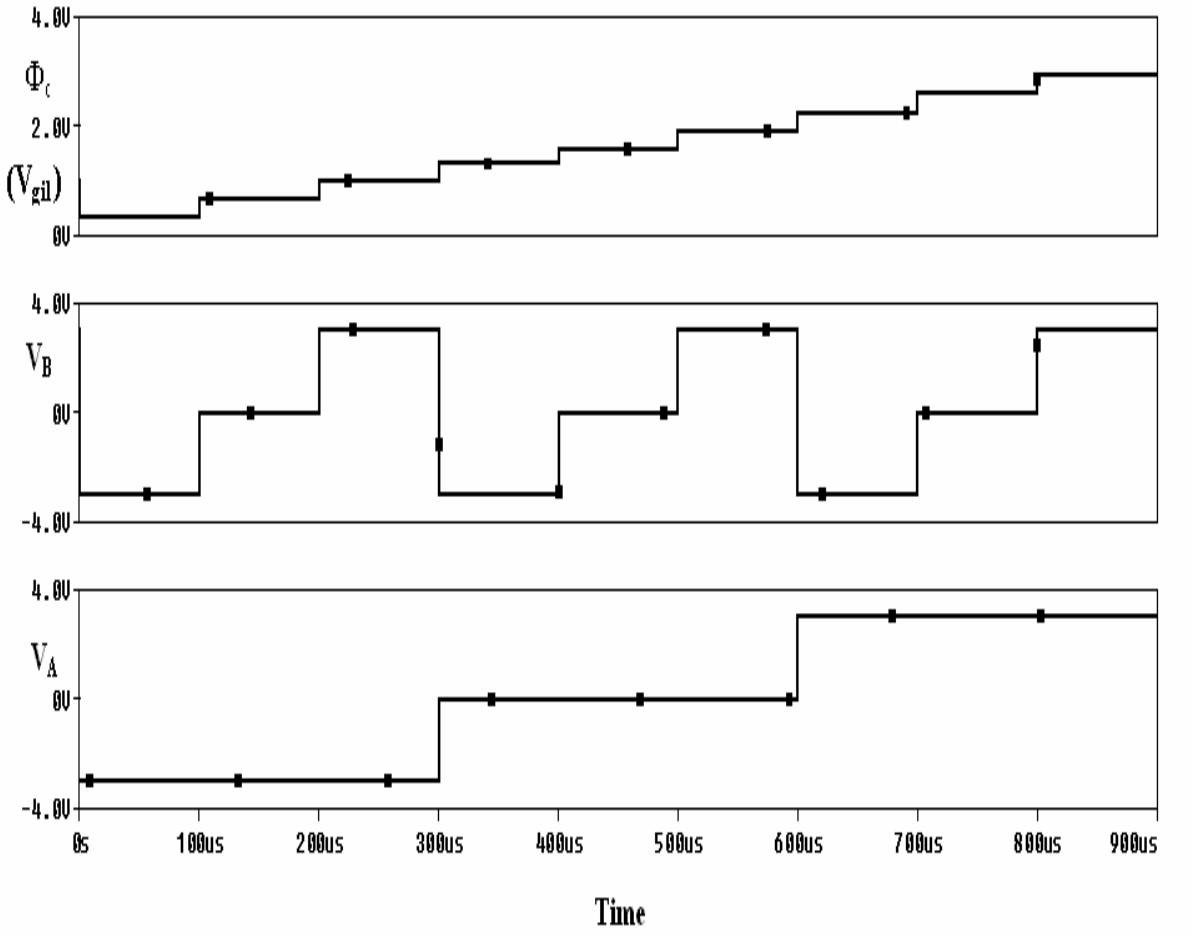


Figure 4.5. Post Layout Simulations for Sign Bit.

Note: V_A, V_B are ternary inputs and Φ_c (V_{gi1}) is the voltage on the floating gate (stage #1).

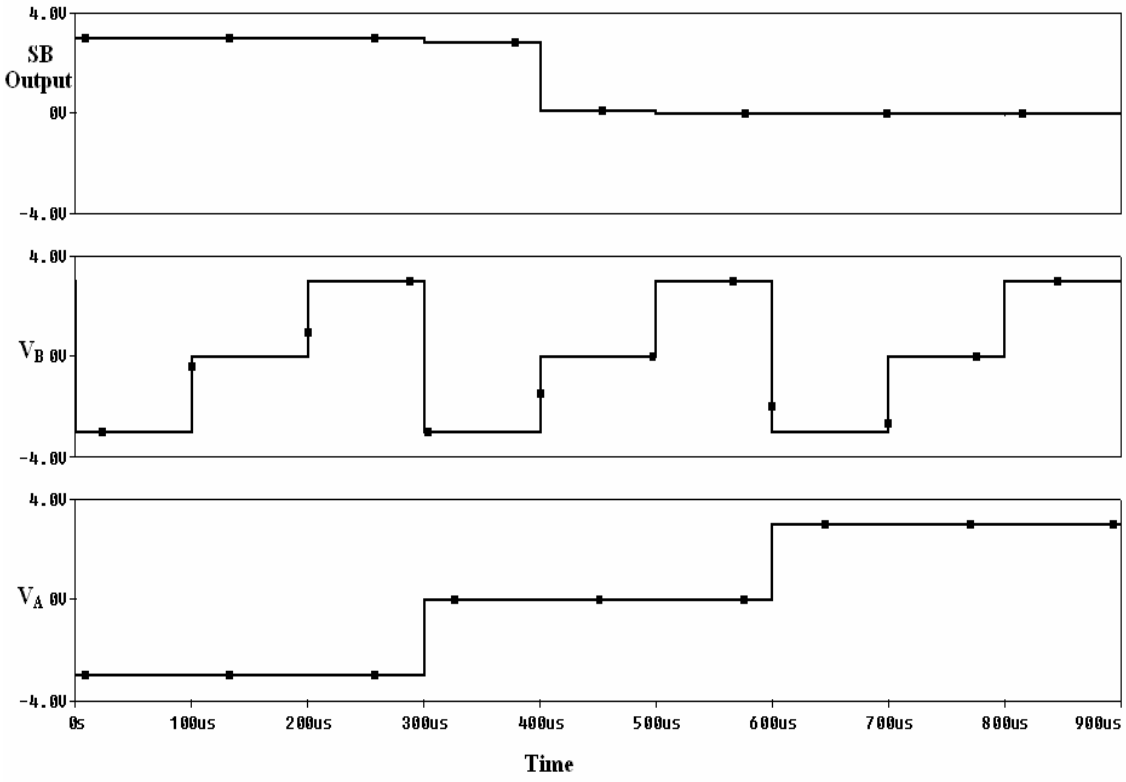


Figure 4.6. Post-Layout Simulations for Sign Bit (SB) With 15 pF Capacitive Load. Note: V_A, V_B are ternary inputs.

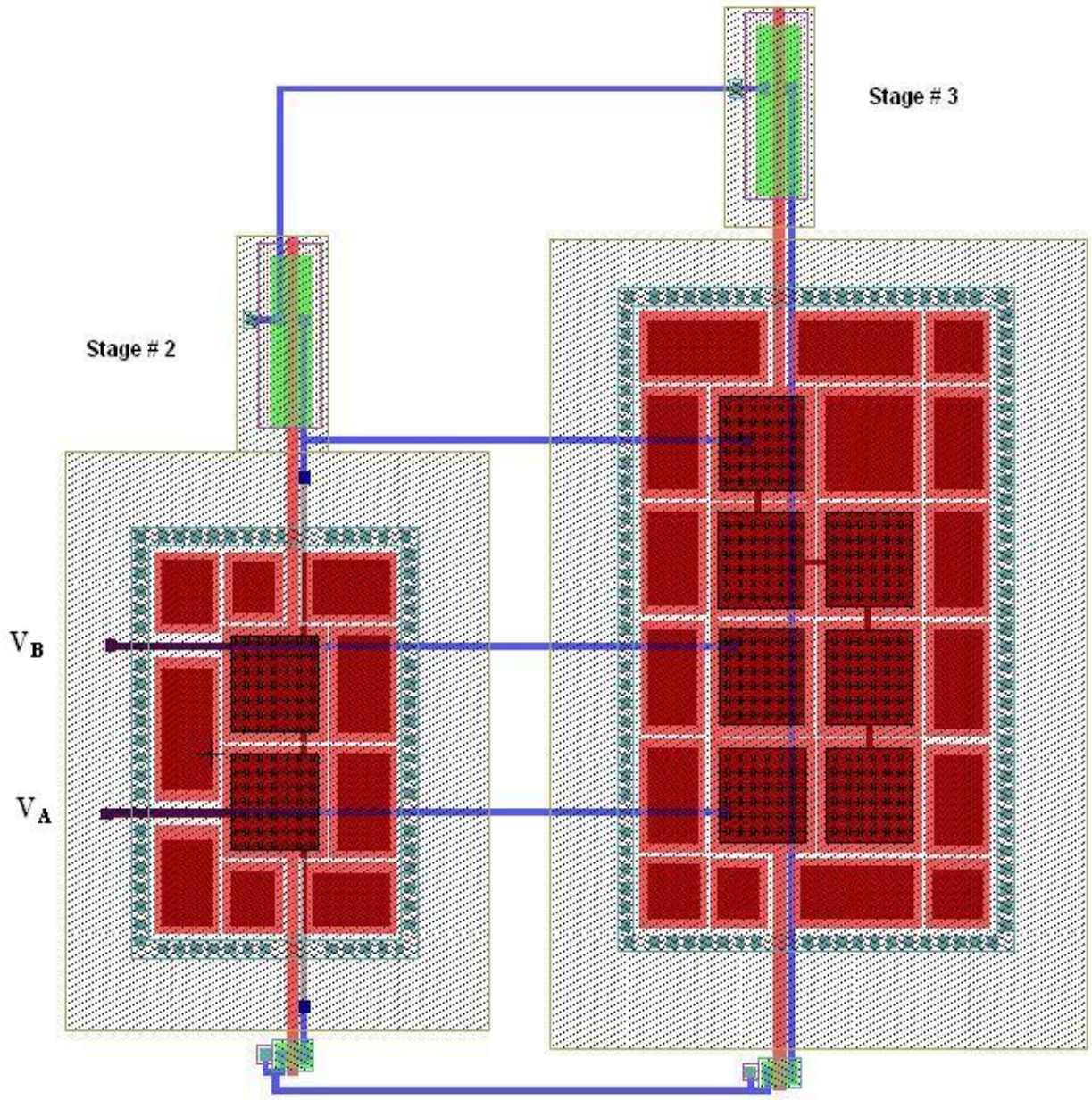


Figure 4.7. Layout for the Most Significant Bit (MSB).

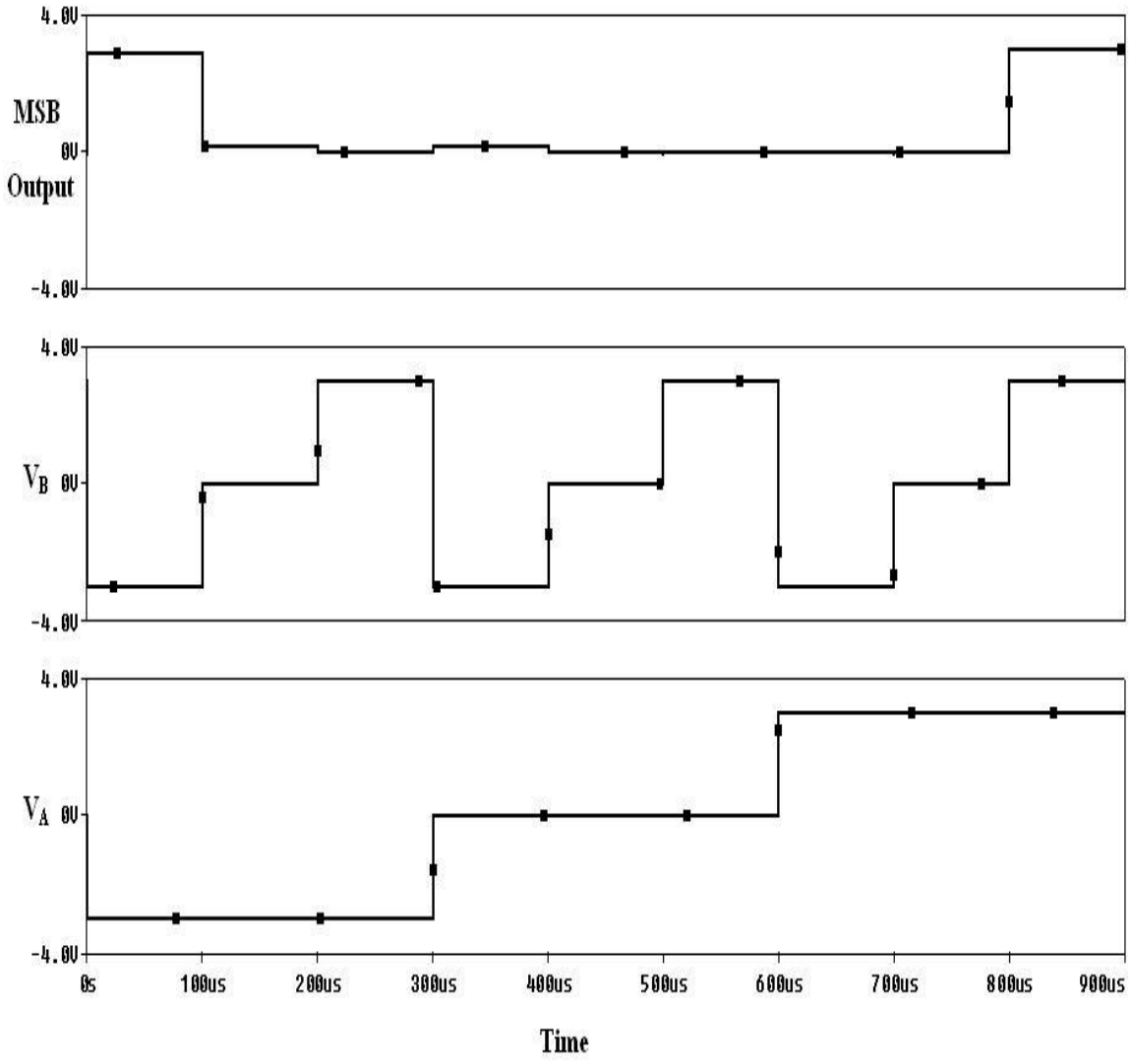


Figure 4.8. Post Layout Output Simulations for Most Significant Bit in No Load condition.

Note: VA, VB are ternary inputs.

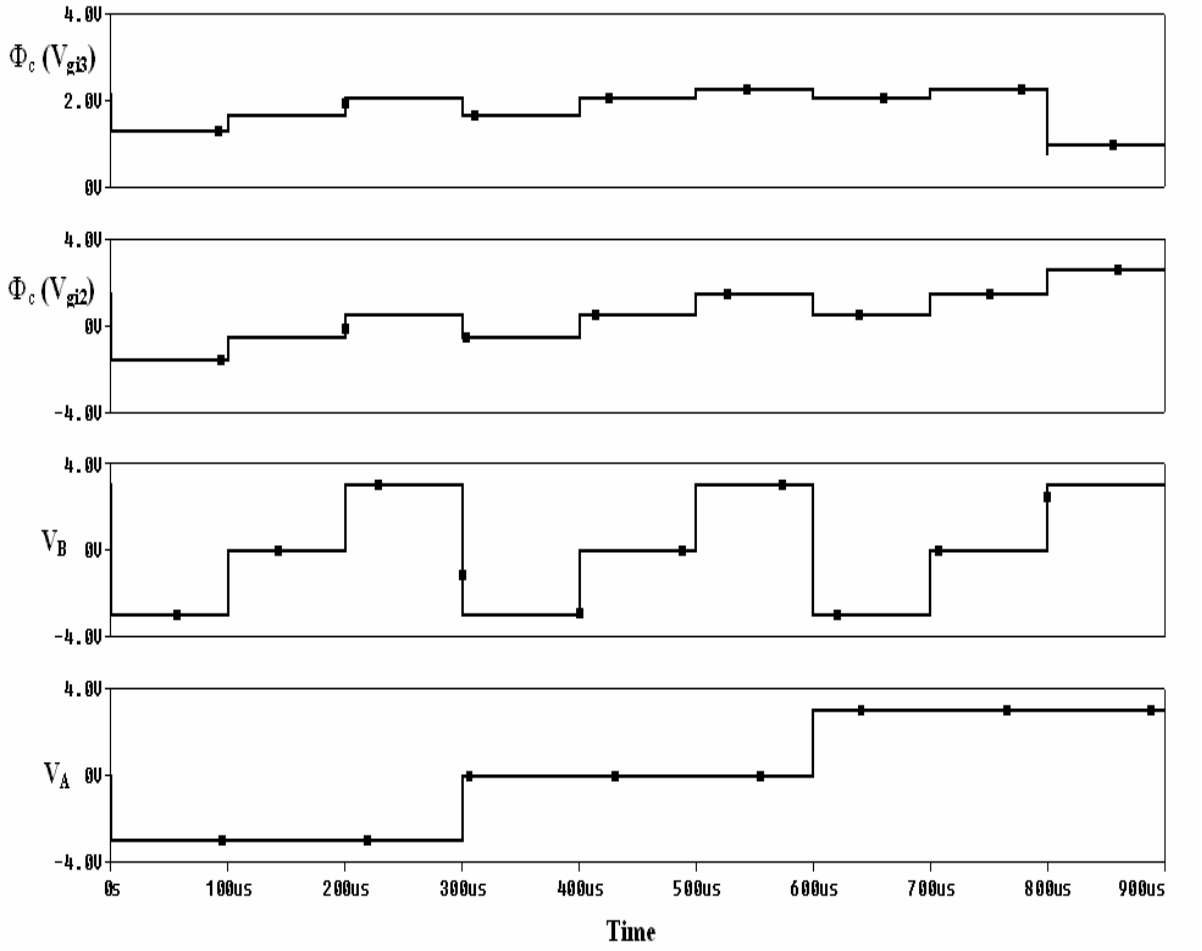


Figure 4.9. Post Layout Simulations for Most Significant Bit.

Note: V_A, V_B are ternary inputs and V_{gi2} and V_{gi3} are the voltages on the floating gates of stage #2 and stage #3, respectively.

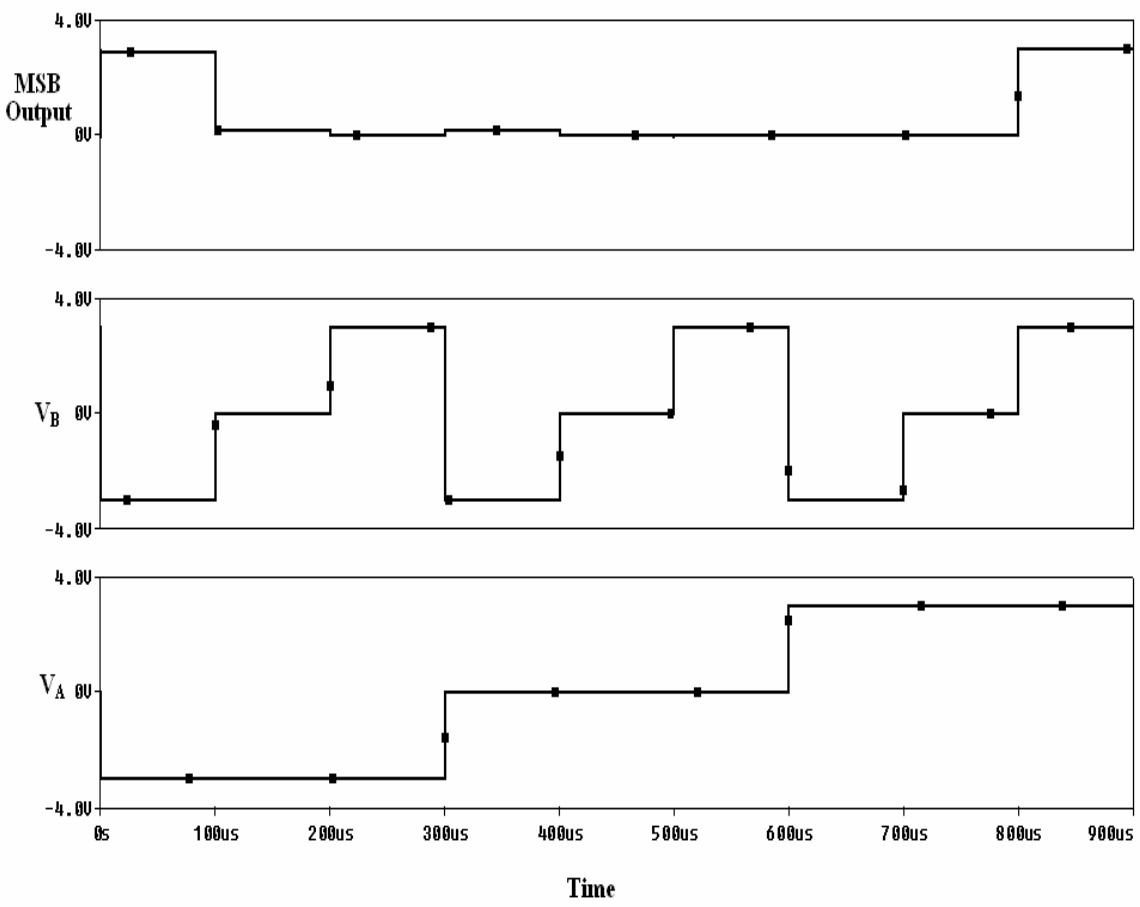


Figure 4.10. Post Layout Output Simulations for MSB With 15 pf Load Capacitance. Note: V_A, V_B are ternary inputs.

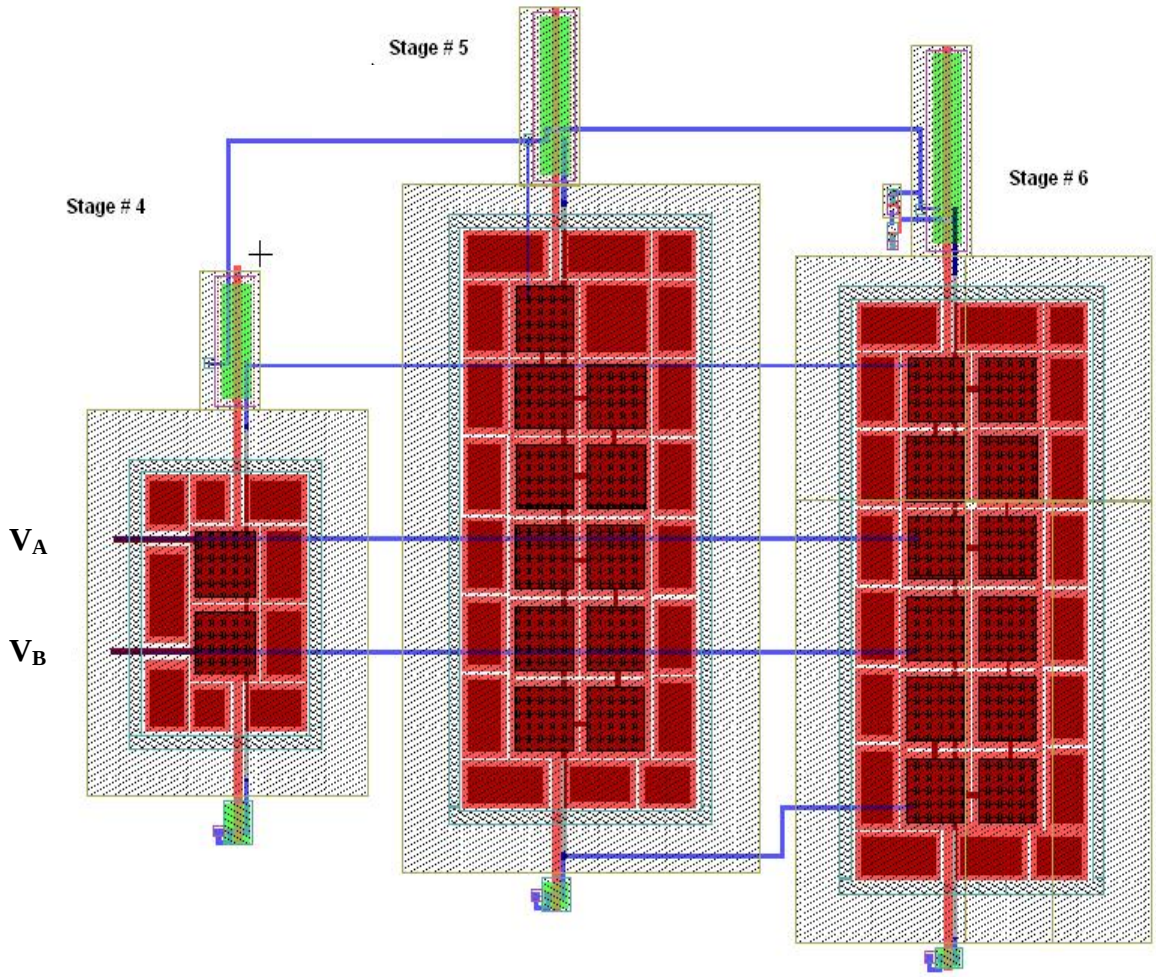


Figure 4.11. Layout for Secondary Significant Bit (SSB).

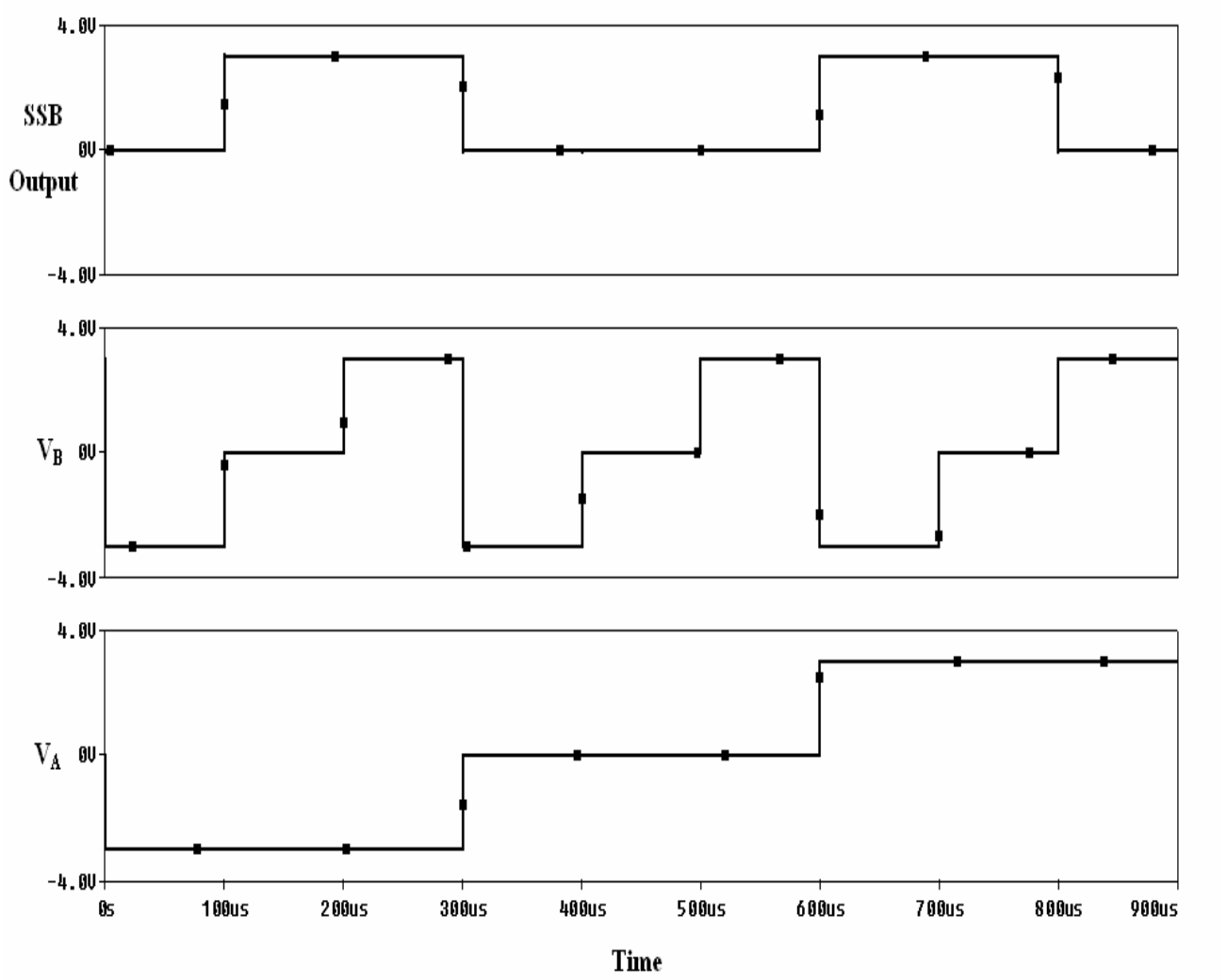


Figure 4.12. Post Layout Output Simulations for Secondary Significant Bit (SSB) in no load condition.

Note: V_A, V_B are ternary inputs.

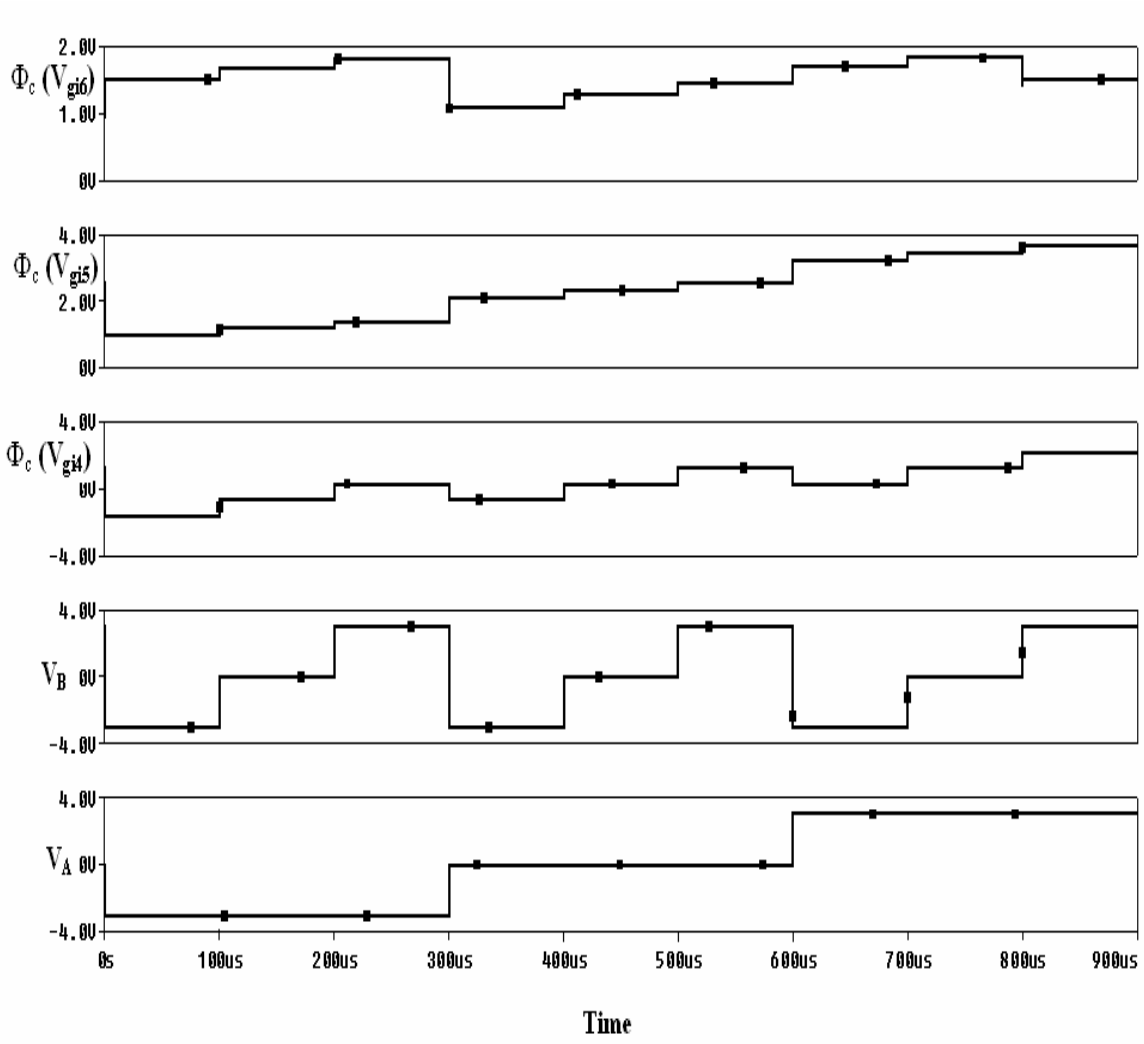


Figure 4.13. Post Layout Simulations for SSB With Gate Voltages.

Note: V_A, V_B are ternary inputs and V_{gi4}, V_{gi5} and V_{gi6} are the voltages on the floating gates of stage #4, stage #5 and stage #6 respectively.

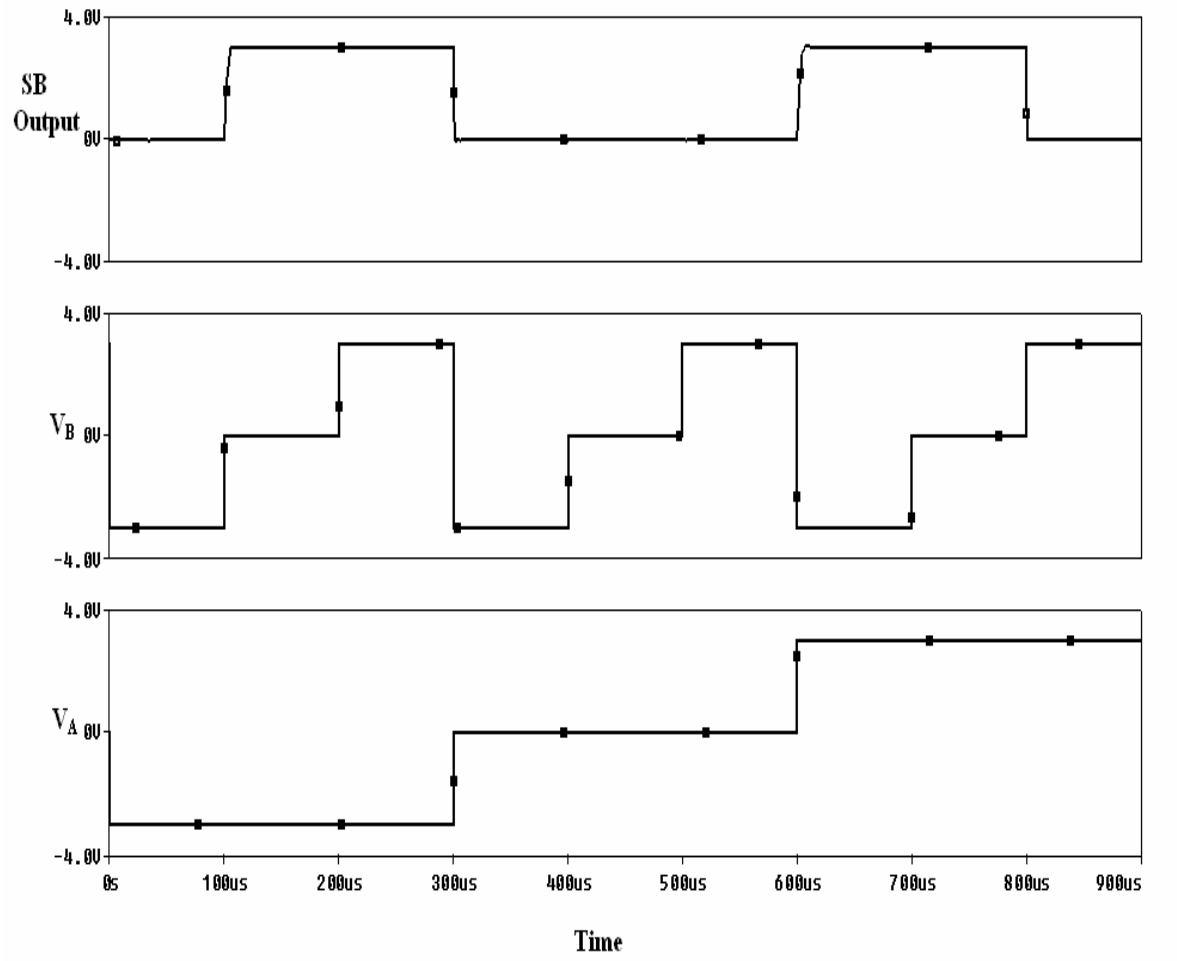


Figure 4.14. Post Layout Output Simulations for SSB With Load Capacitance of 15 pf. Note: V_A, V_B are ternary inputs.

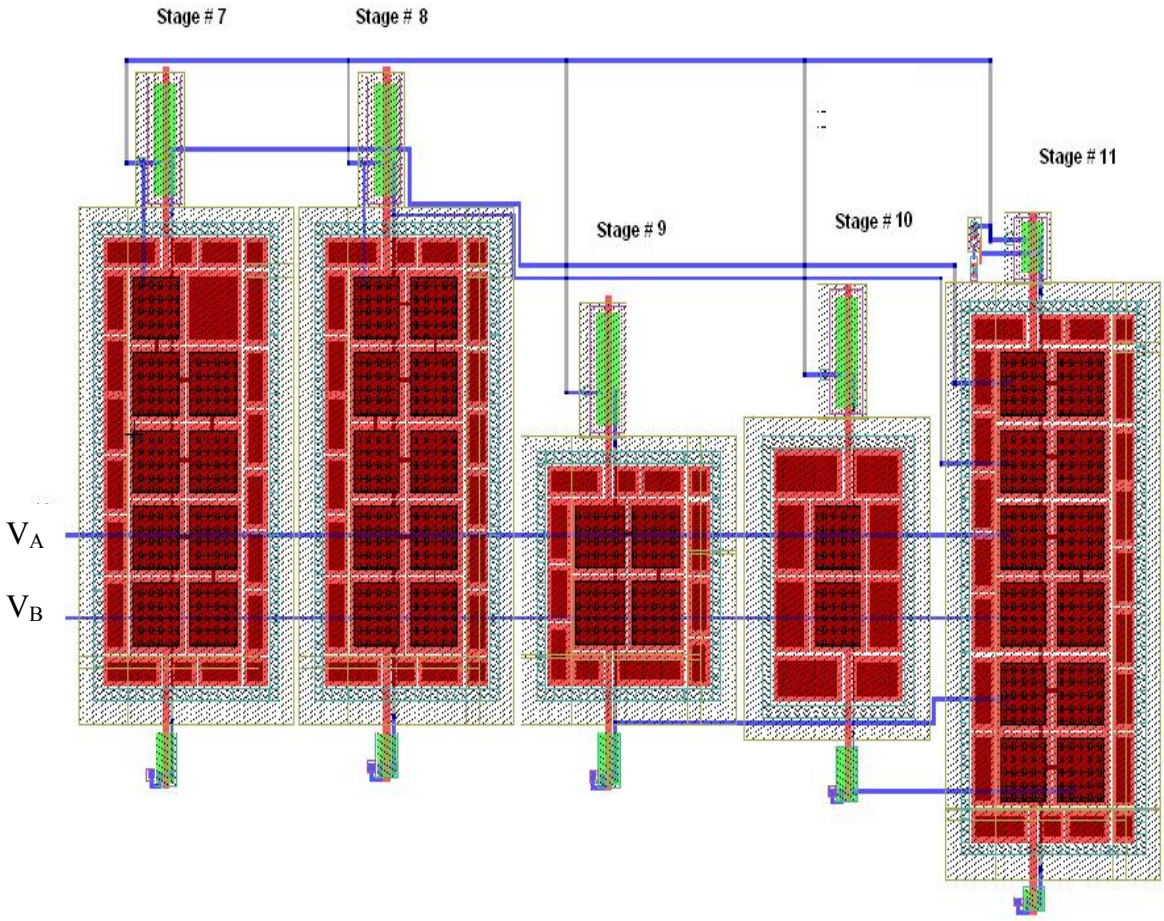


Figure 4.15. Layout for Least Significant Bit (LSB).

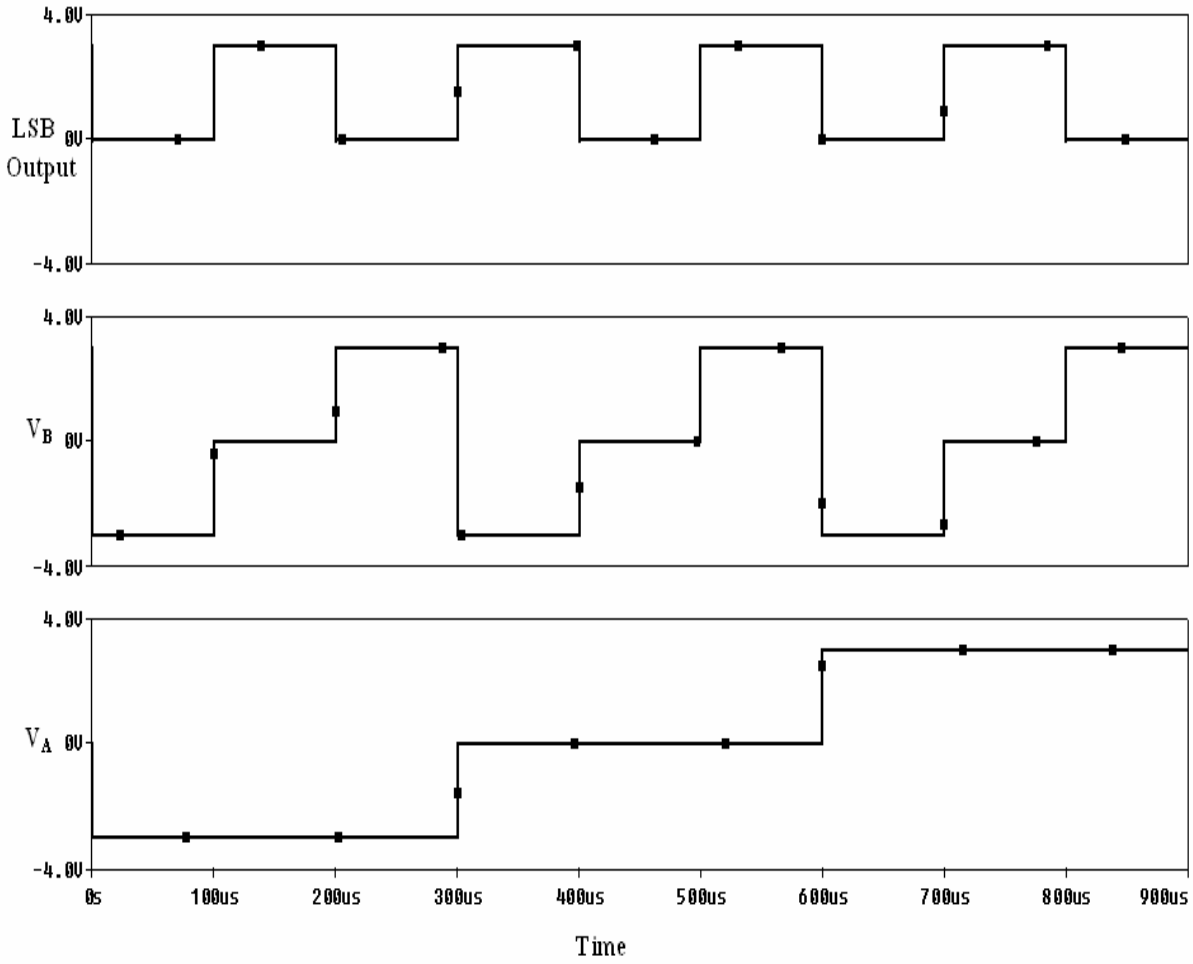


Figure 4.16. Post Layout Output Simulations for Least Significant Bit (LSB) in No Load Condition.

Note: V_A, V_B are ternary inputs.

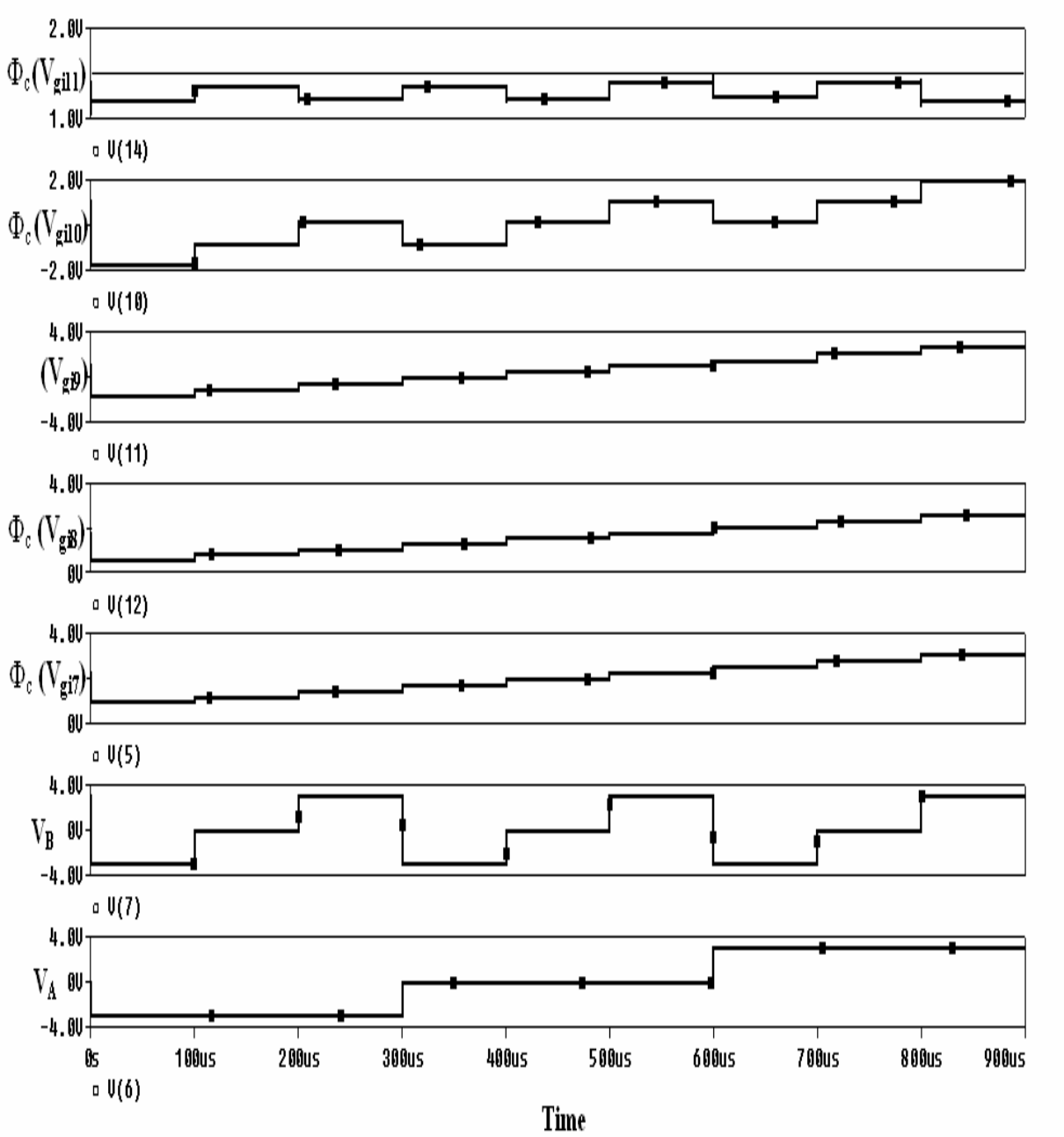


Figure 4.17. Post Layout Simulations for LSB With Gate Voltages.

Note: V_A, V_B are ternary inputs and V_{gi7} to V_{gi11} are the voltages on the floating gates (stage #7 to stage #11).

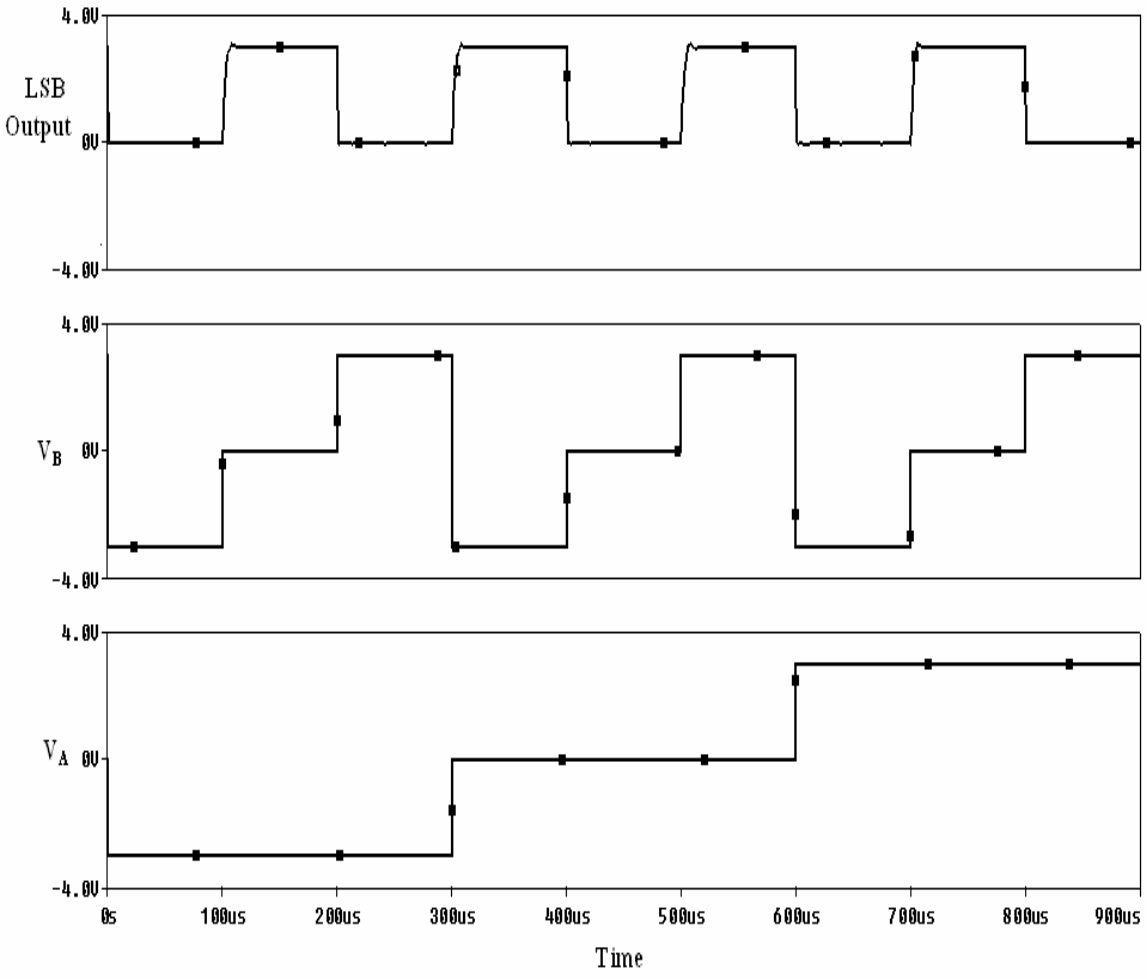


Figure 4.18. Post Layout Output Simulations for LSB With a Load Capacitance of 15 pf. Note: V_A, V_B are ternary inputs.

Table 4.1. Delays for Different Stages of the Ternary to Binary Conversion

Logic Level Transition (Ternary Logic)	SB		MSB		SSB		LSB	
	Sim. (µs)	Exp. (µs)	Sim. (µs)	Exp. (µs)	Sim. (µs)	Exp. (µs)	Sim. (µs)	Exp. (µs)
-4 to -3 (-1-1) to (-1 0)	-	-	1.160	3.6	6.970	11.2	9.180	14.6
-3 to -2 (-1 0) to (-1 1)	-	-	-	-	-	-	2.041	8.3
-2 to -1 (-1 1) to (0 -1)	-	-	-	-	3.825	9.7	10.204	23.9
-1 to 0 (0 -1) to (0 0)	1.632	-	-	-	-	-	2.070	8.3
0 to 1 (0 0) to (0 1)	-		-	-	-	-	11.225	31.4
1 to 2 (0 1) to (1 -1)	-	-	-	-	7.570	14.3	1.020	7.6
2 to 3 (1 -1) to (1 0)	-	-	-	-	-	-	8.163	14.0
3 to 4 (1 0) to (1 1)	-	-	-	-	-	-	3.069	8.8

Note: Sim: Simulation
Exp: Experimental

comparison with simulated values. The maximum propagation delay time is 23.9 μs. Table 4.2 summarizes measured and simulated bit outputs from the designed ternary-to-binary bit converter. The measured bits are obtained from Figures 4.23 to 4.38.

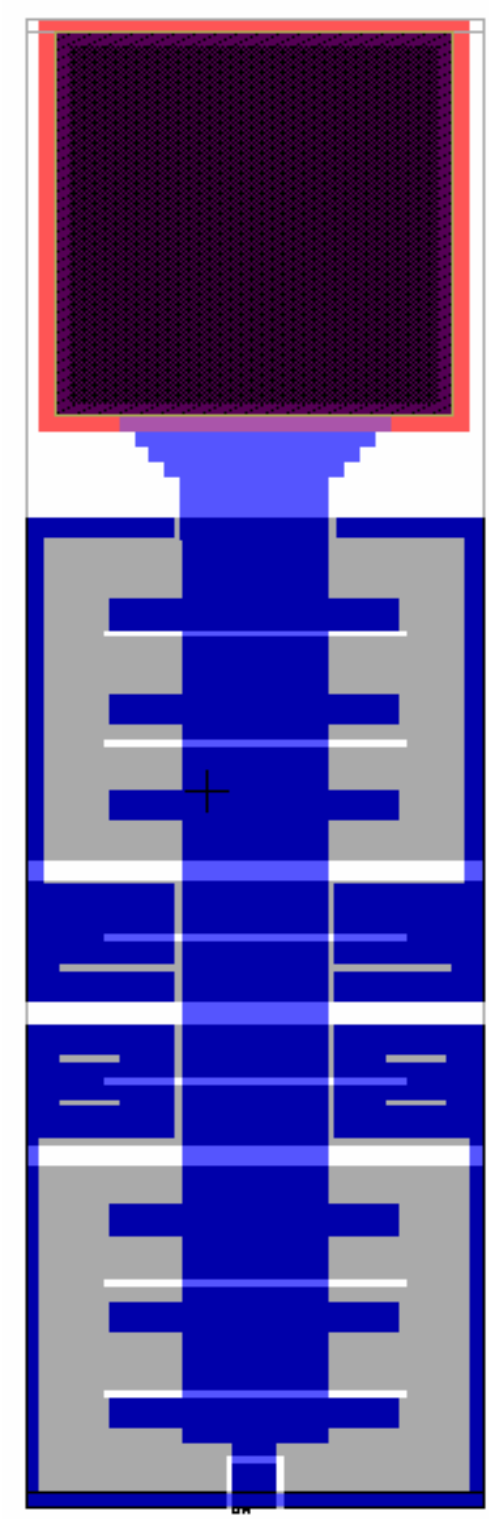


Figure 4.19. Layout of an Analog Pad.

Table 4.2. Pin Number Allocation

1	SB	Output for SB
2	-	-
3	SB VGI1	Stage #1 Floating gate Input
4	-	-
5	MSB	Output for MSB
6	MSB VGI 2	Stage #3 Floating gate Input
7	MSB VOUT1	Output of stage # 2
8	MSB VGI 1	Stage #2 Floating gate Input
9	LSB	Output for LSB
10	LSB VOUT5	Output of stage # 11
11	LSB VGI 5	Stage #11 Floating gate Input
12	LSB VGI4	Stage #10 Floating gate Input
13	LSB VGI3	Stage #9 Floating gate Input
14	LSB VGI2	Stage #8 Floating gate Input
15	LSB VGI 1	Stage #7 Floating gate Input
16	LSB VOUT 2	Output of stage # 8
17	LSB VOUT 1	Output of stage # 7
18	LSB VOUT 3	Output of stage # 9
19	LSB VOUT 4	Output of stage # 10
20	V_A	Ternary Input
21	VDD	Supply 3V
22	V_B	Ternary Input
23	SSB VGI 1	Stage #4 Floating gate Input
24	SSB VGI 2	Stage #5 Floating gate Input
25	SSB VOUT1	Output of stage # 4
26	SSB VOUT 2	Output of stage # 5
27	SSB VGI 3	Stage #6 Floating gate Input
28	SSB VOUT 3	Output of stage # 6
29	-	-
30	SSB	Output for SSB
31-39	-	-
40	VSS	Supply 0V

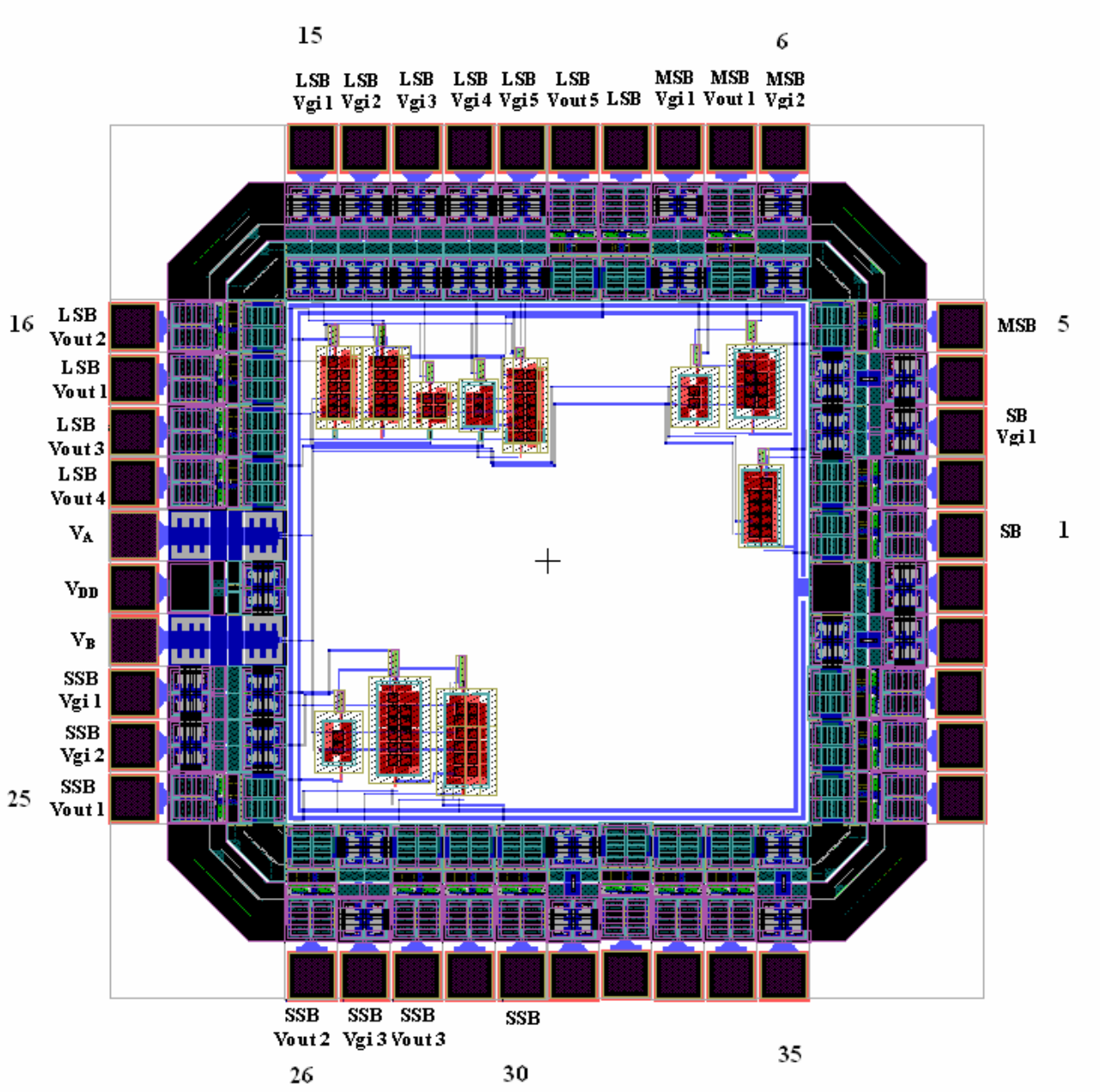


Figure 4.20. Ternary-to-Binary Converter Chip.

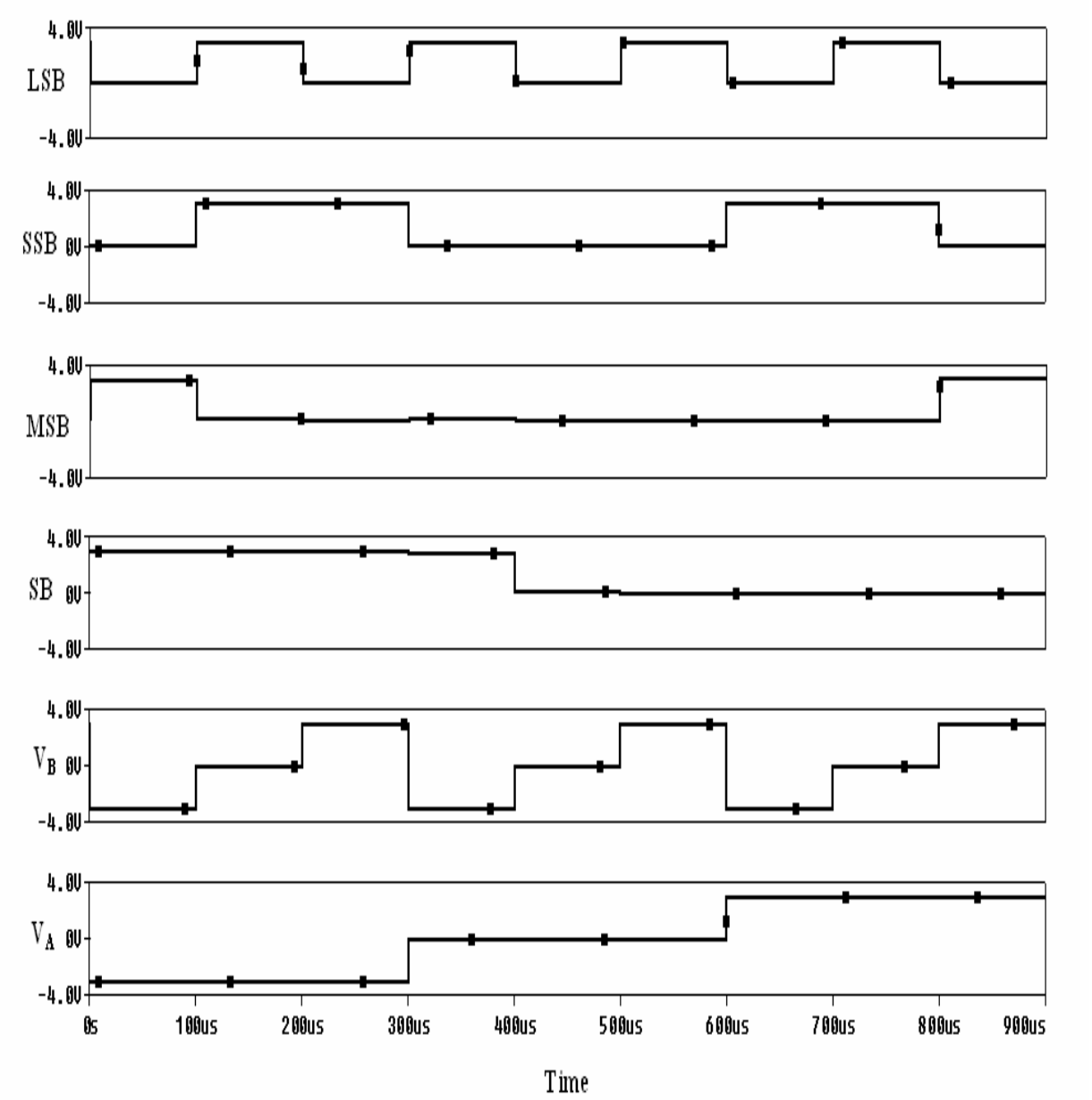


Figure 4.21. Post-Layout Output Simulation of the Ternary to Binary Converter.

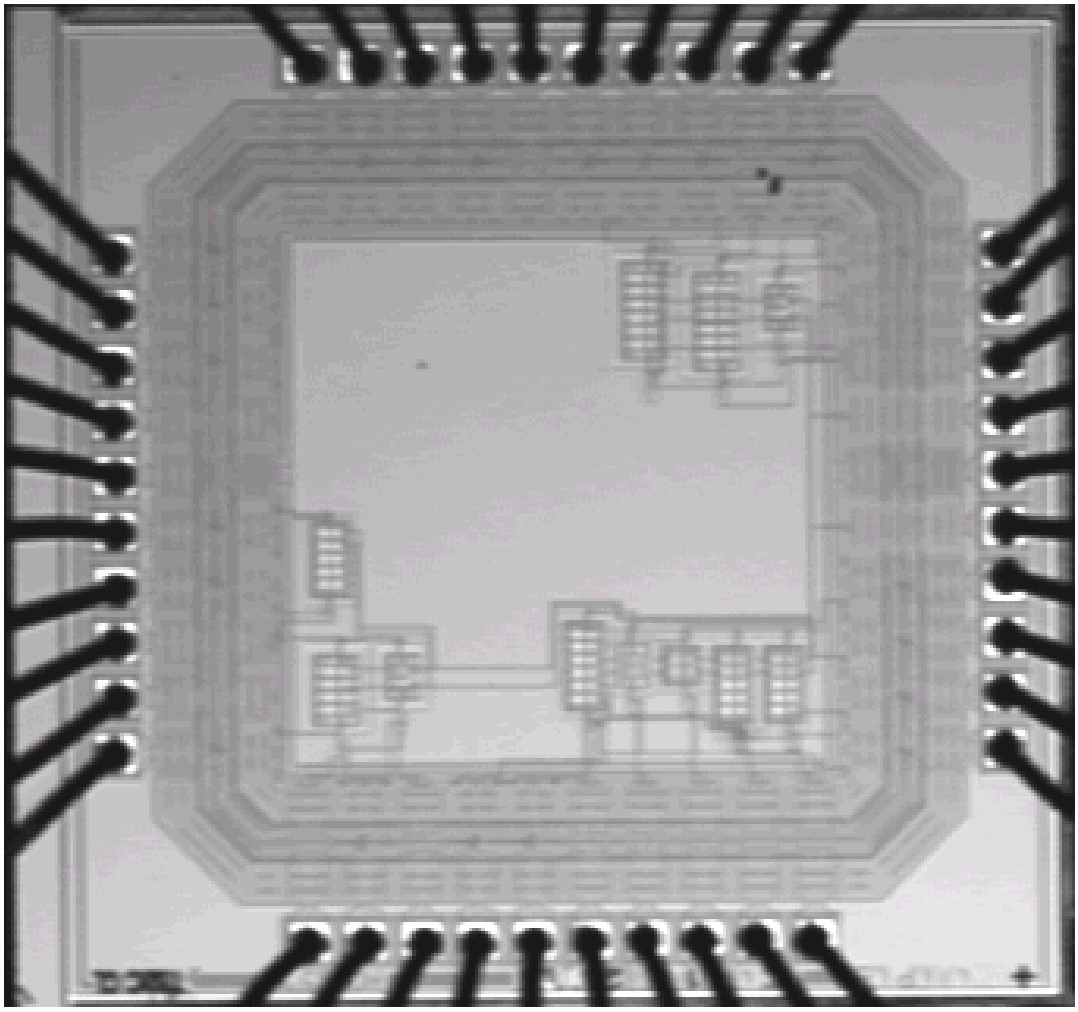
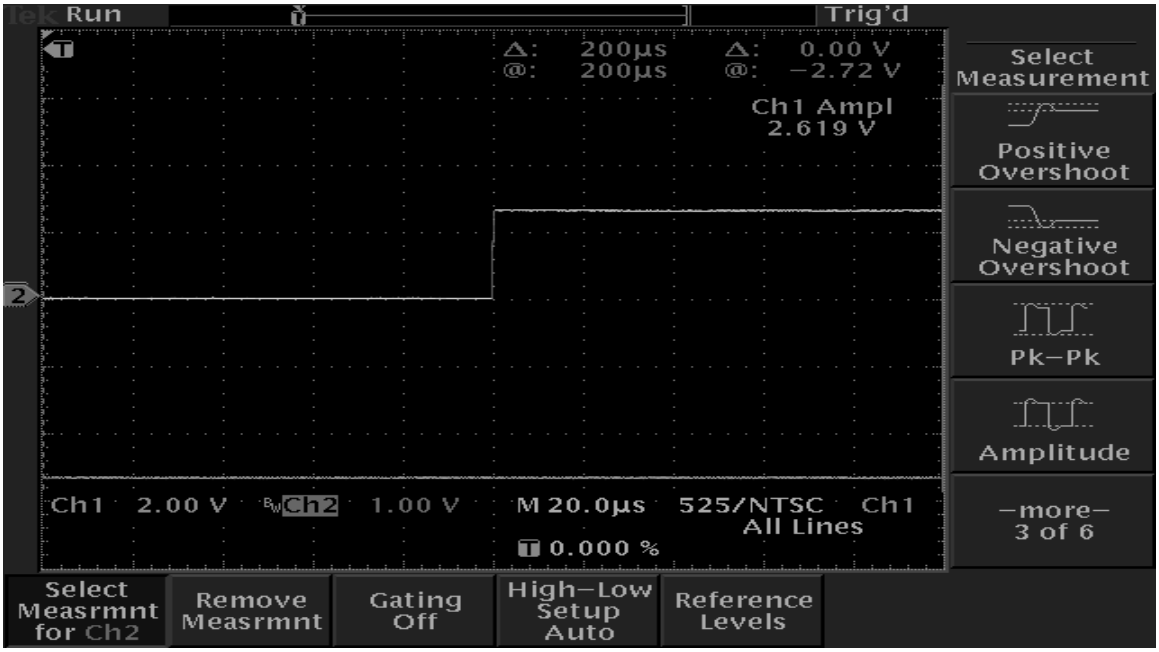


Figure 4.22. Microphotograph of the Ternary-to-Binary Converter Chip

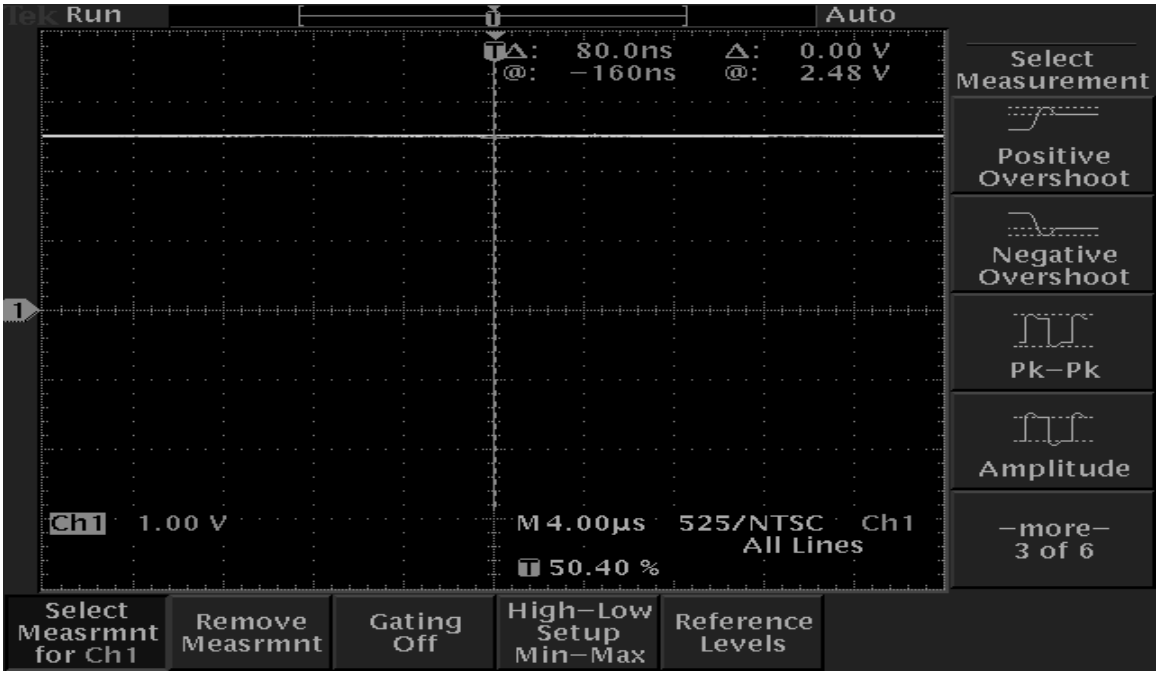
Table 4.3. Experimental Output for Various Bits

Va	Vb	SB		MSB		SSB		LSB	
		Sim	Exp	Sim	Exp	Sim	Exp	Sim	Exp
-1	0	1	1	0	0	1	1	1	1
-1	1	1	1	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	1
1	0	0	0	0	0	1	1	1	1
1	1	0	0	1	1	0	0	0	0
0	-1	1	1	0	0	0	0	1	1
1	-1	0	0	0	0	1	1	0	0

Note: Sim: Simulated
Exp: Experimental
-1, 0, 1 correspond to the voltage levels -3V, 0V, 3V, respectively.

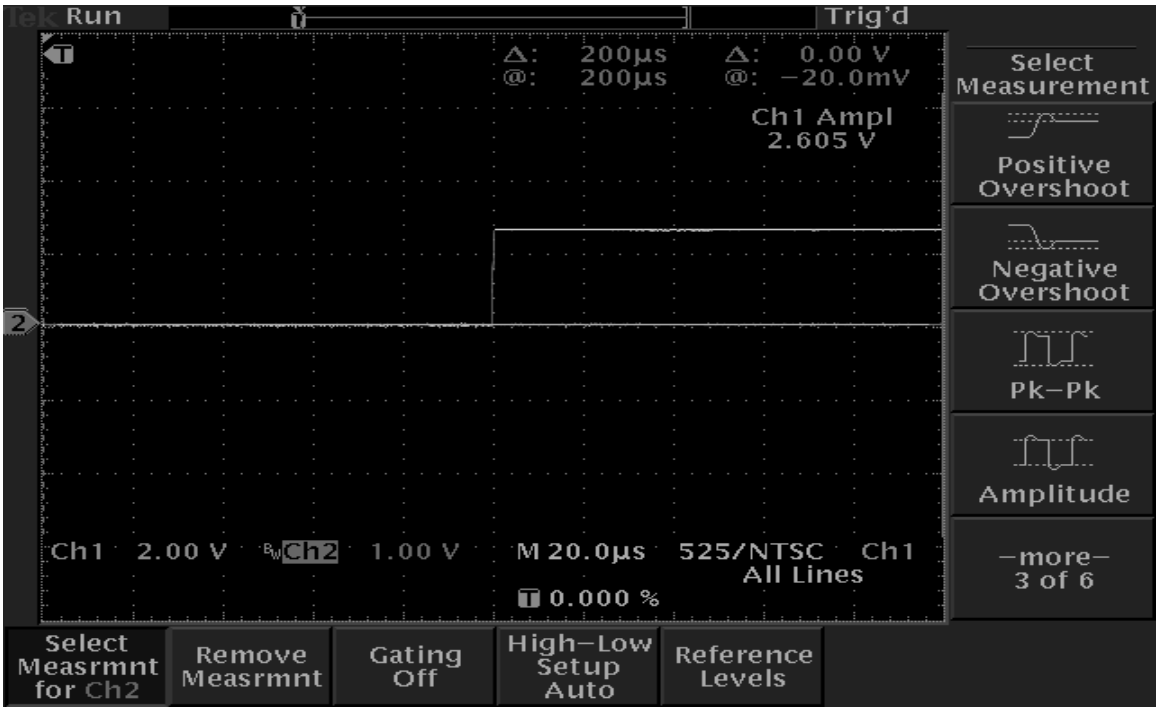


(a)

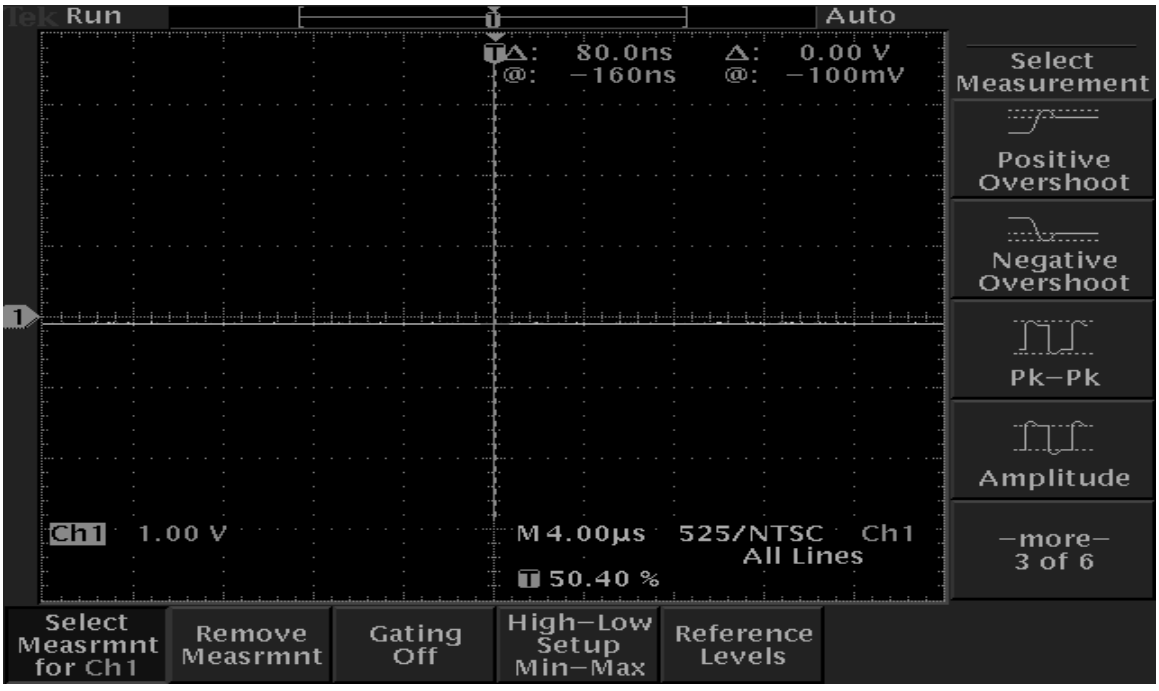


(b)

Figure 4.23. Measured SB Waveforms. (a) V_A is at -3V and V_B Varying from 0 V to3 V and (b) Output Waveform for Input Condition Shown in (a).

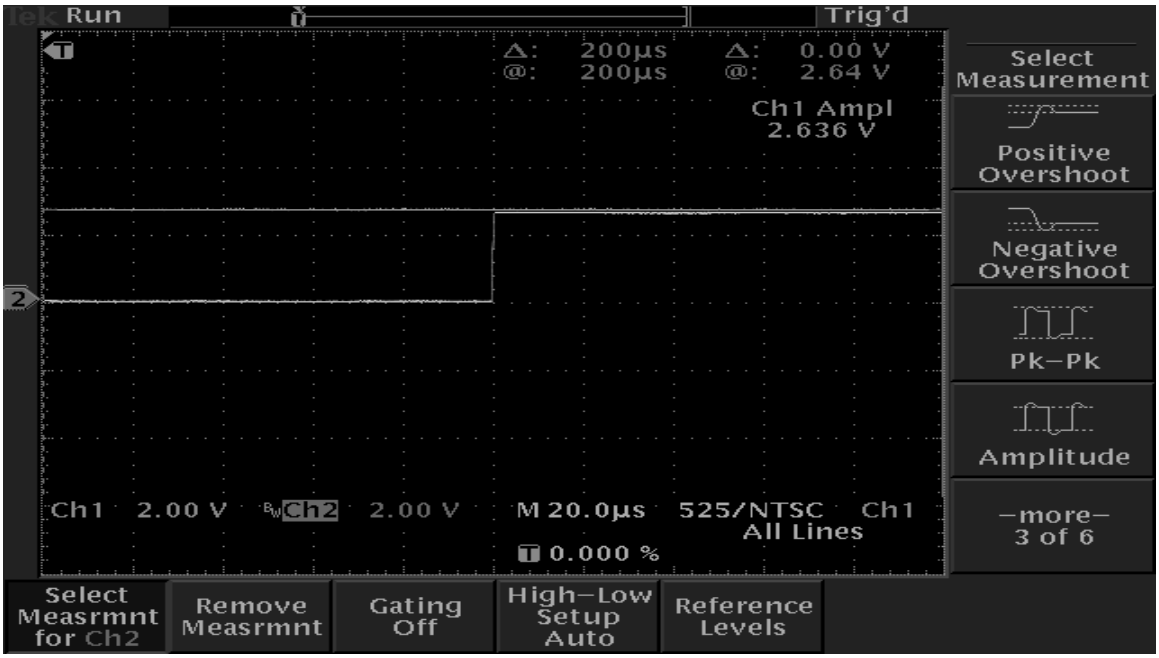


(a)

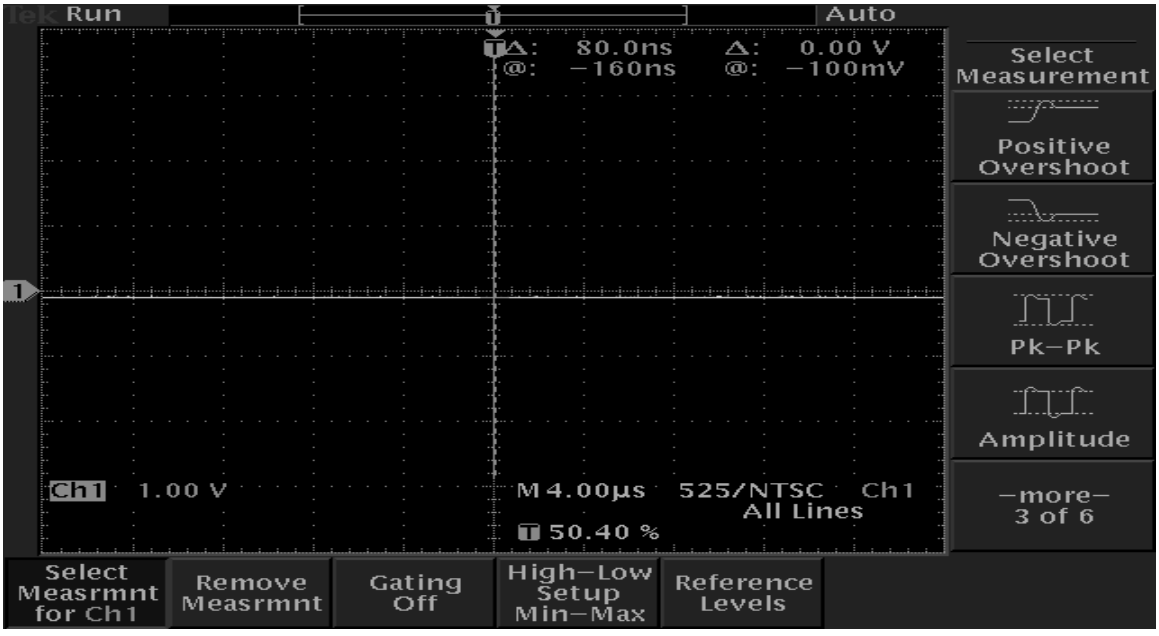


(b)

Figure 4.24. Measured SB Waveforms. (a) V_A is at 0 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

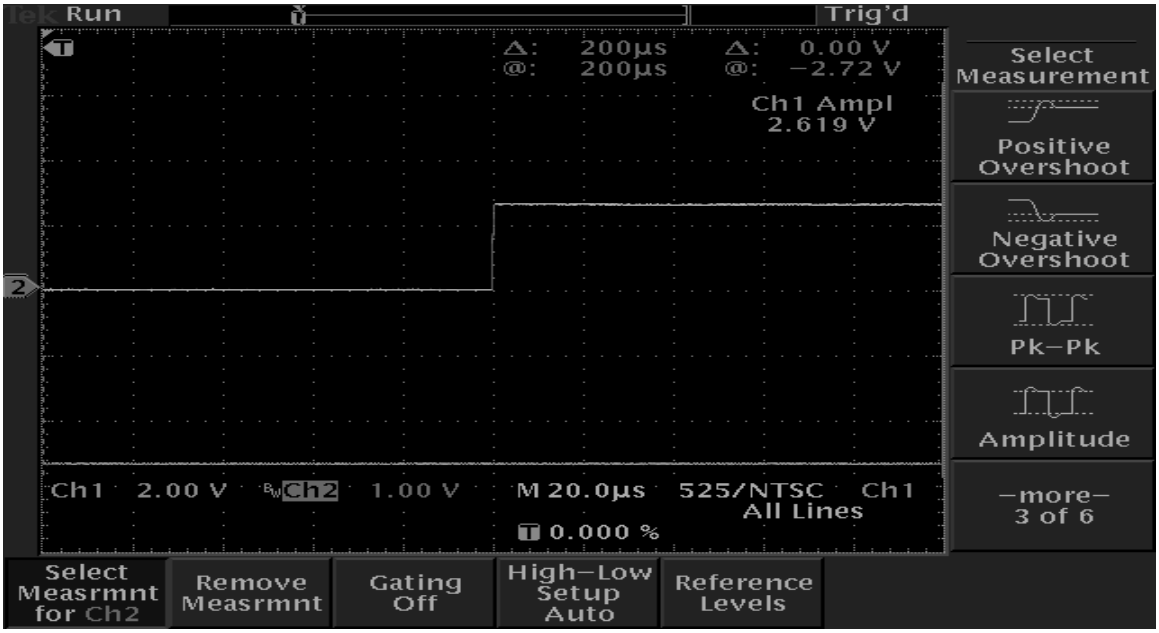


(a)

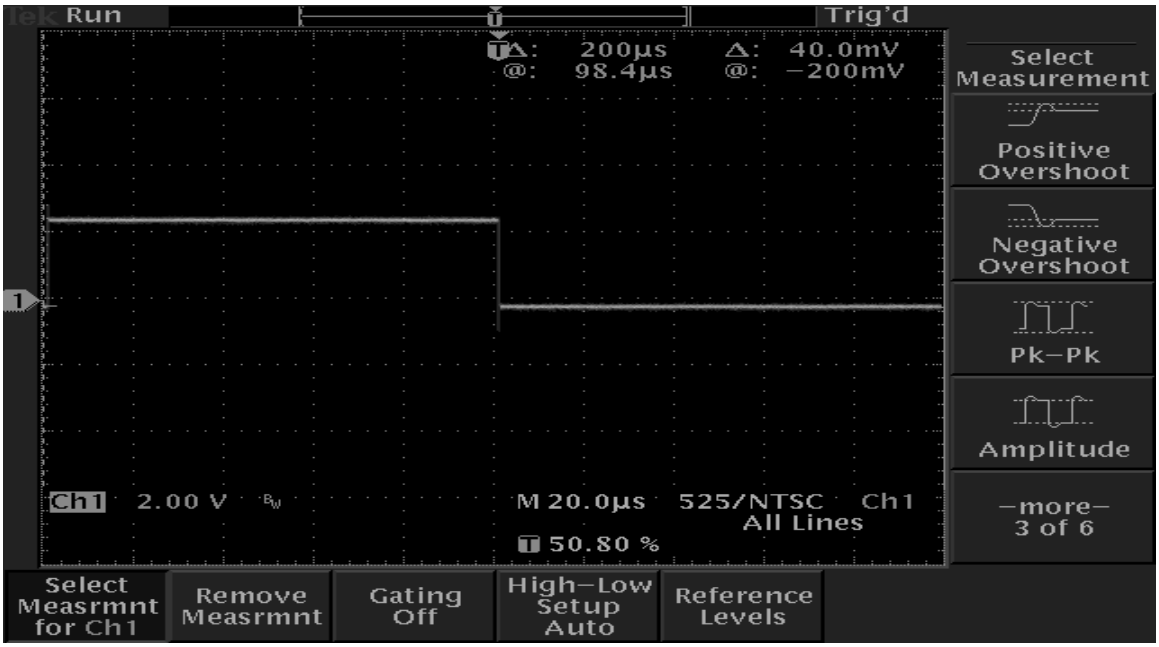


(b)

Figure 4.25. Measured SB Waveforms. (a) V_A is at 3 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

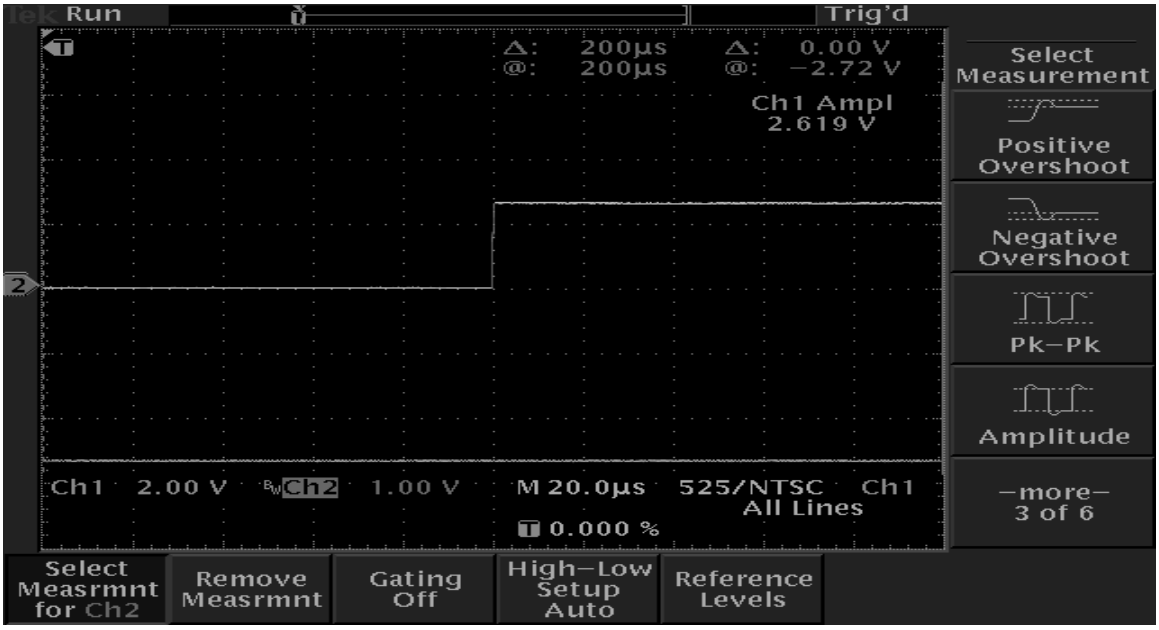


(a)

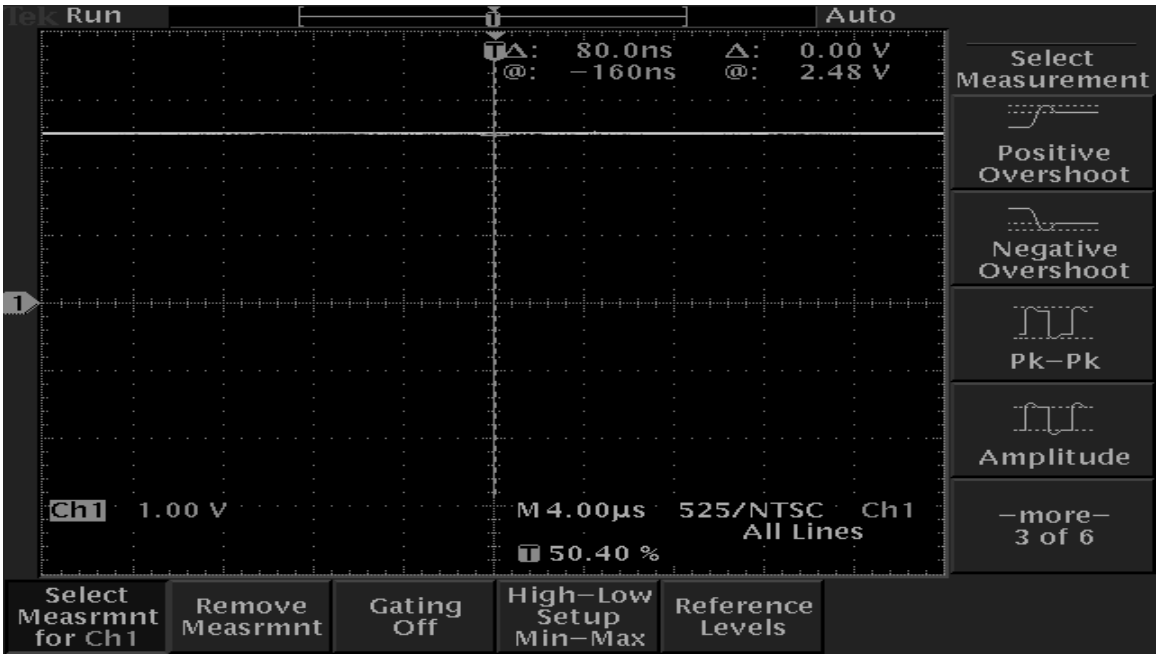


(b)

Figure 4.26. Measured SB Waveforms. (a) V_B is at -3 V and V_A Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

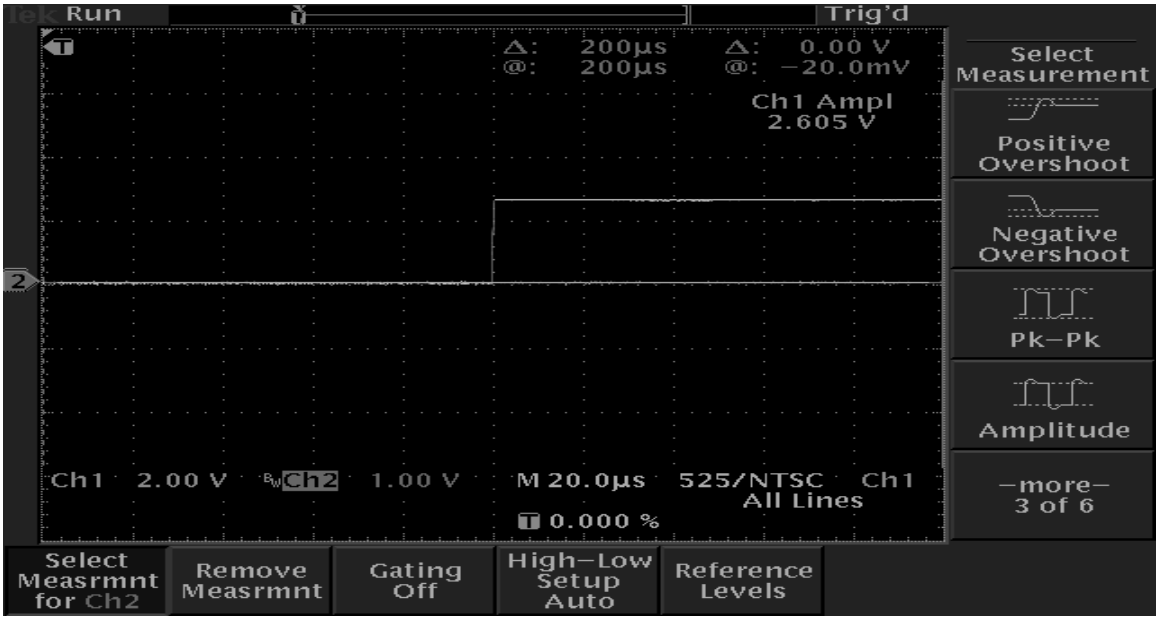


(a)

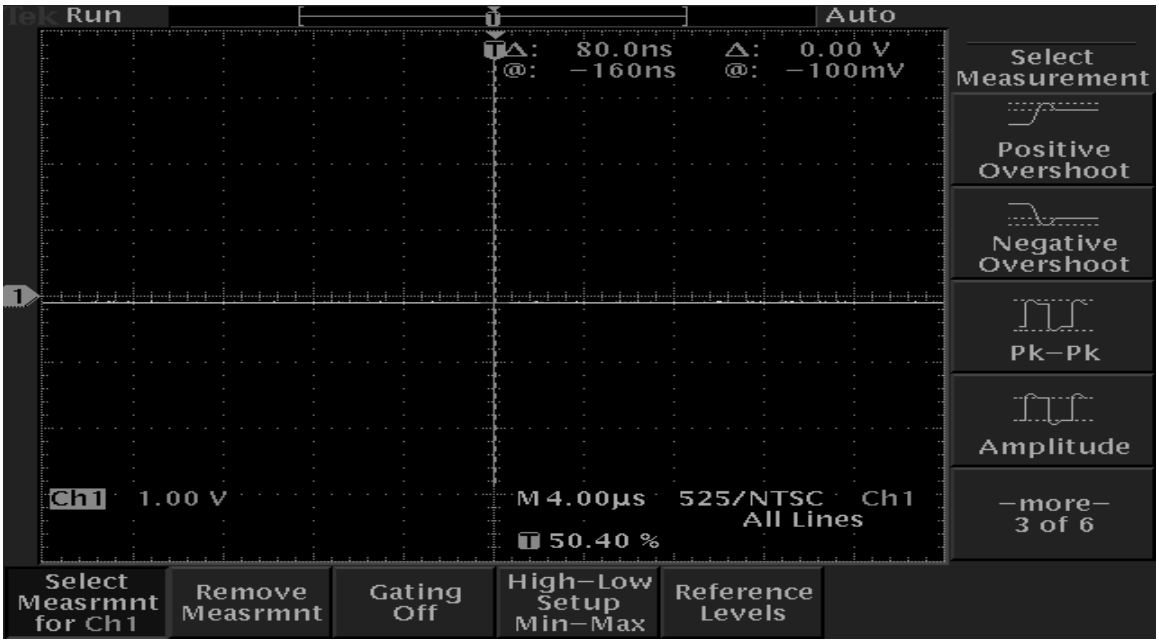


(b)

Figure 4.27. Measured MSB Waveforms. (a) V_A is at -3 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

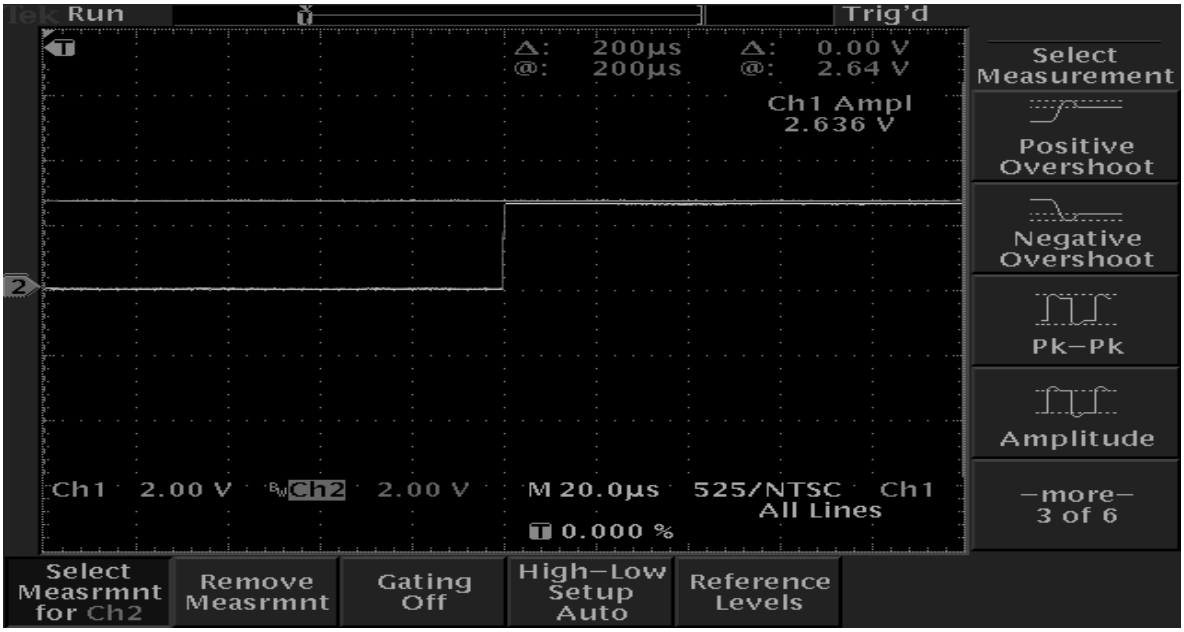


(a)

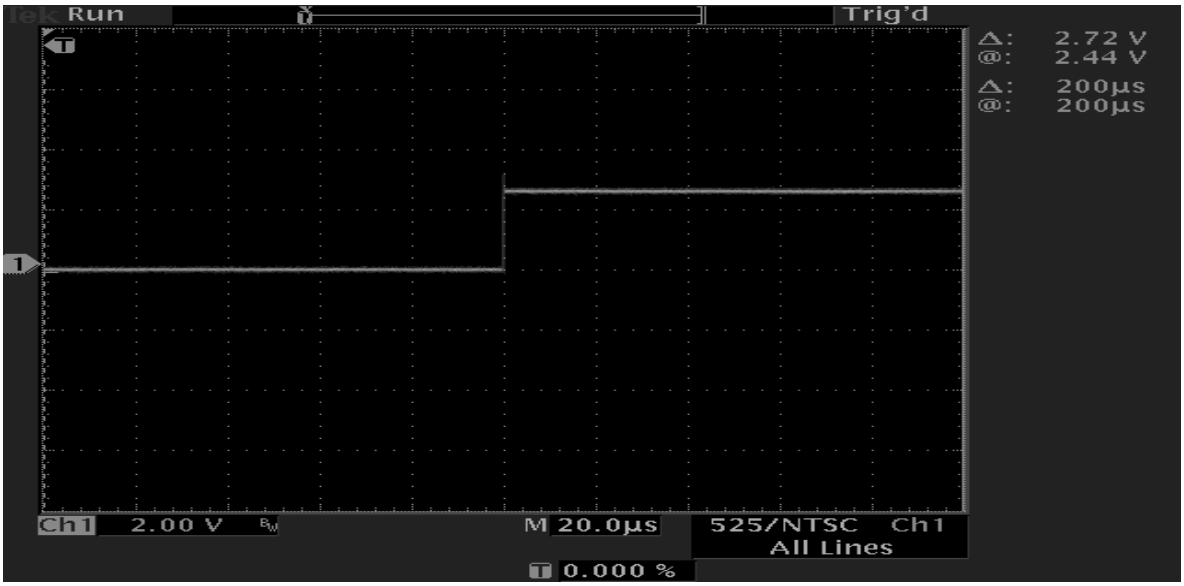


(b)

Figure 4.28. Measured MSB Waveforms. (a) V_A is at 0 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

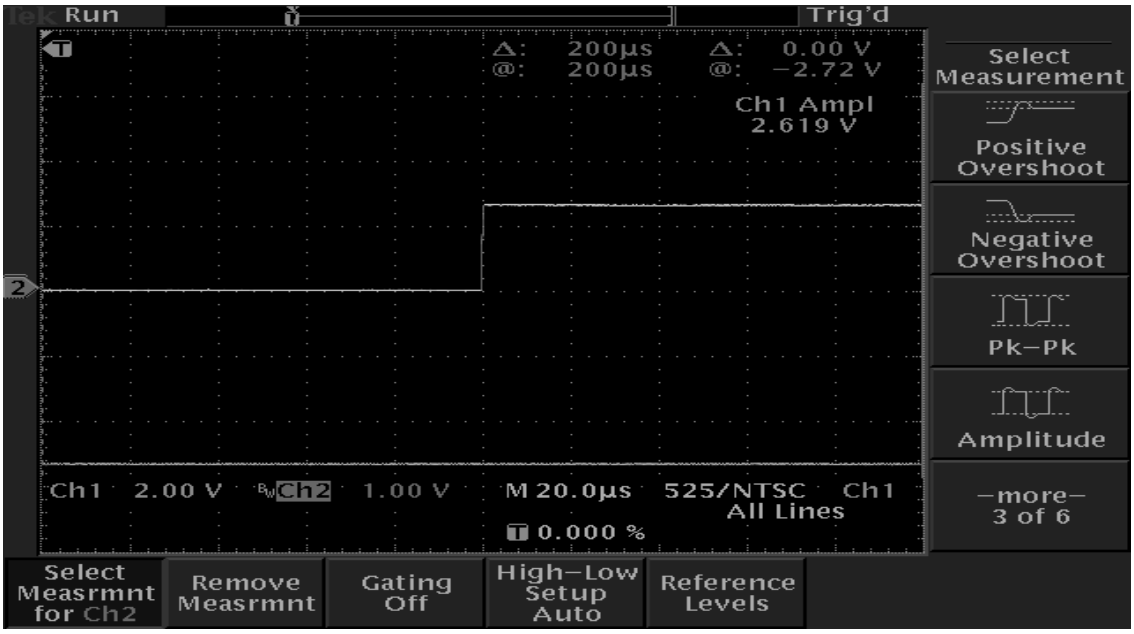


(a)

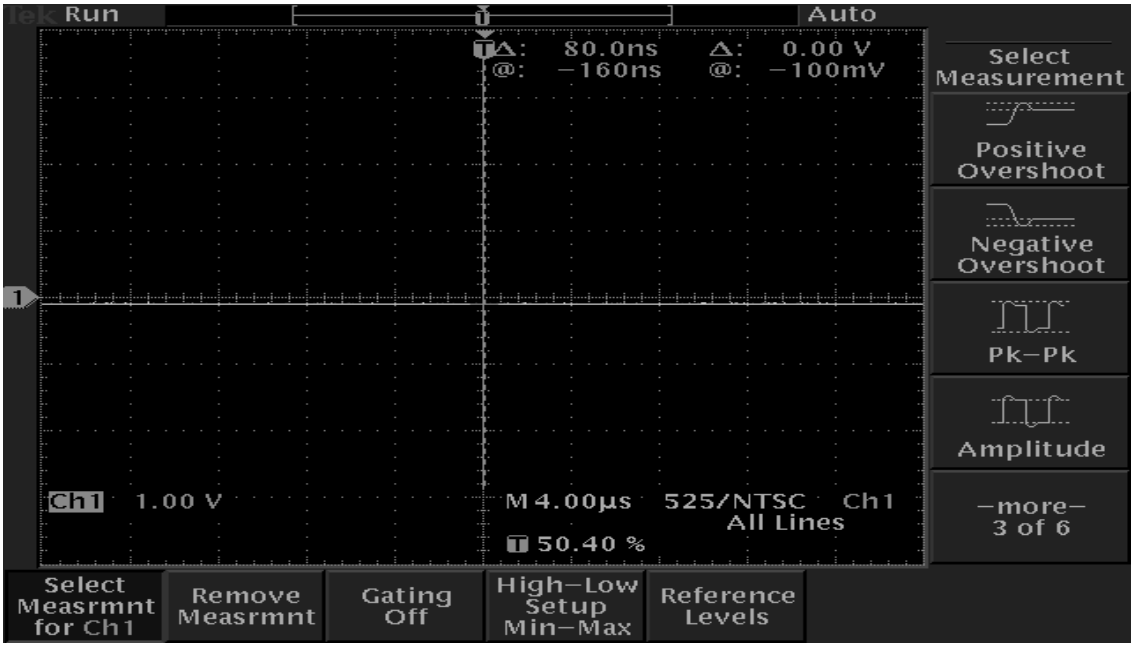


(b)

Figure 4.29. Measured MSB Waveforms. (a) V_A is at 3 V and V_B Varying from 0 V to 3 Vand (b) Output Waveform for Input Condition Shown in (a).

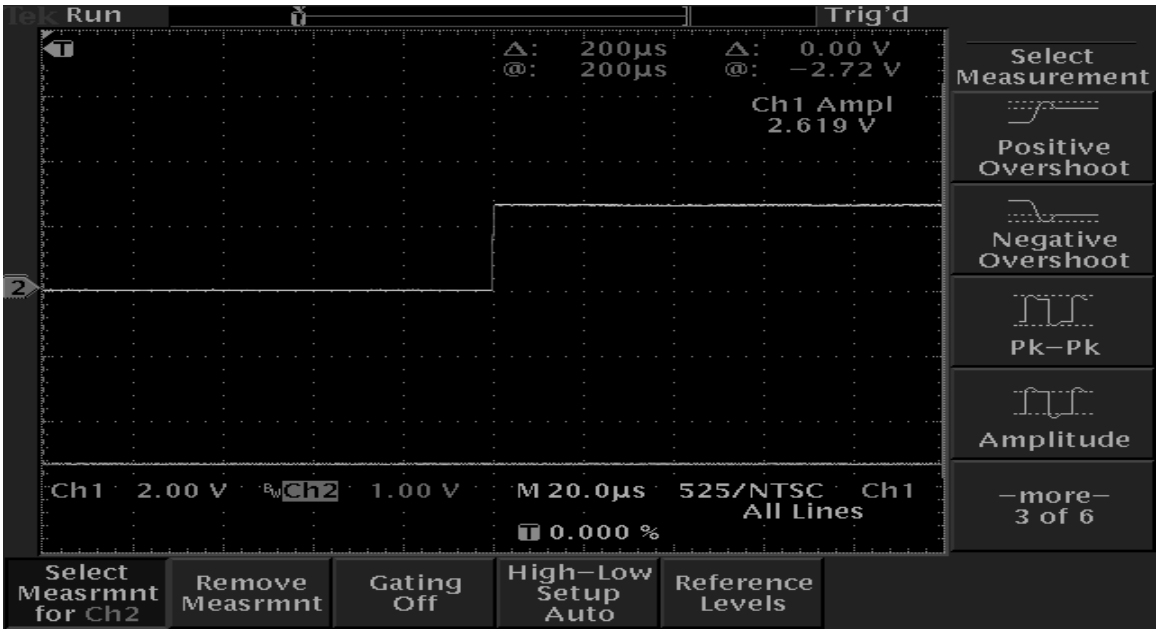


(a)

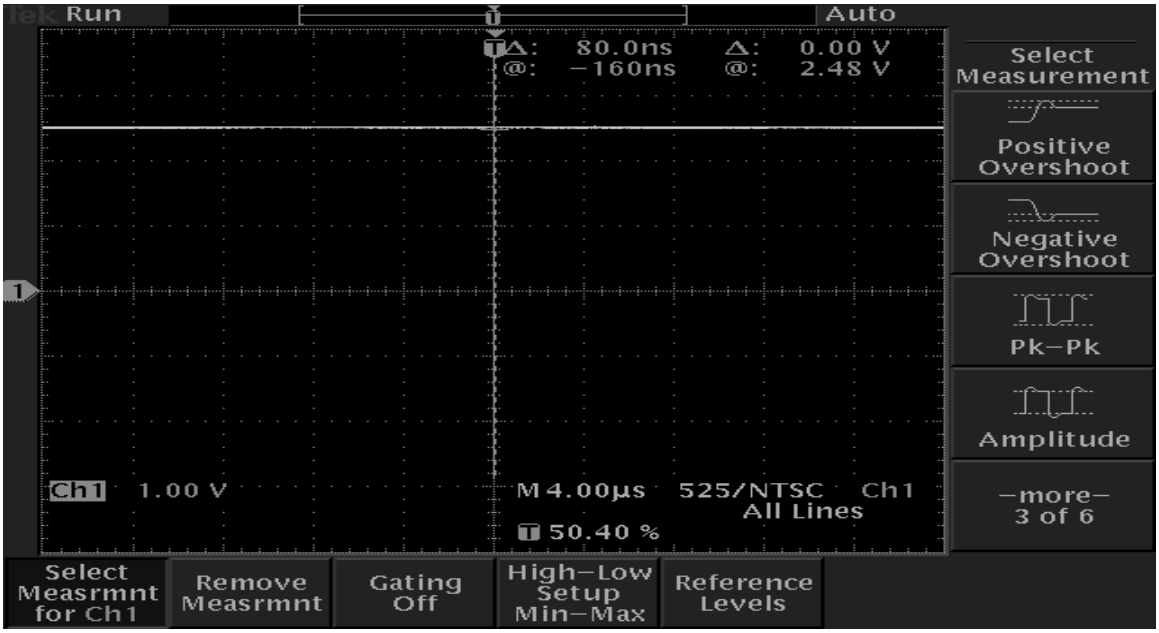


(b)

Figure 4.30. Measured MSB Waveforms. (a) V_B is at -3 V and V_A Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

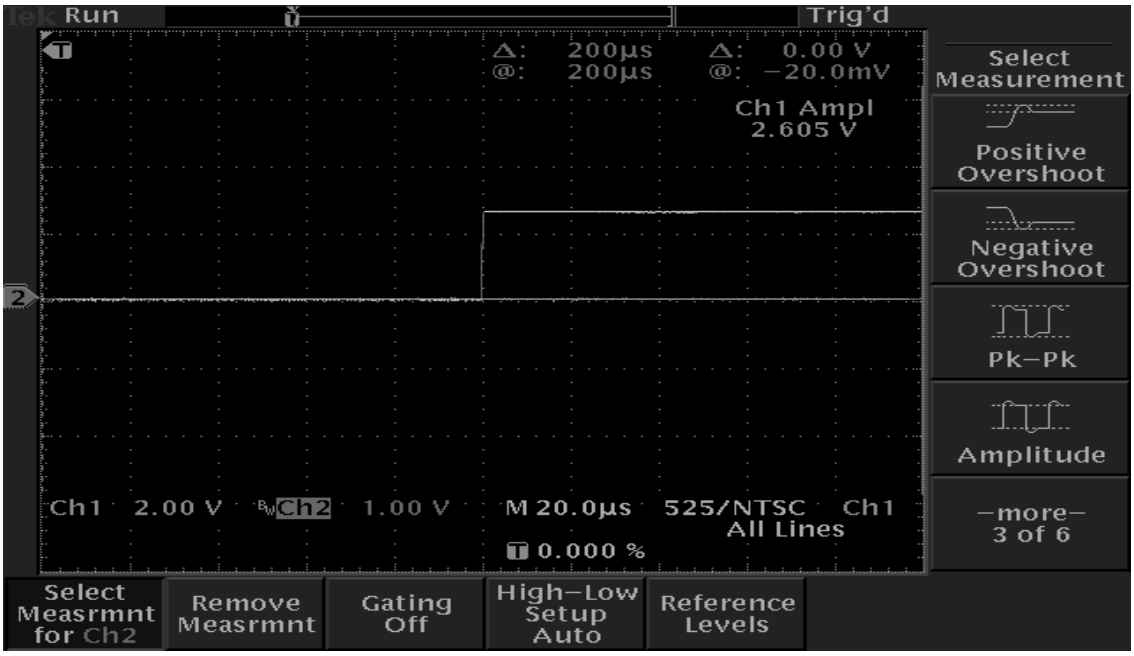


(a)

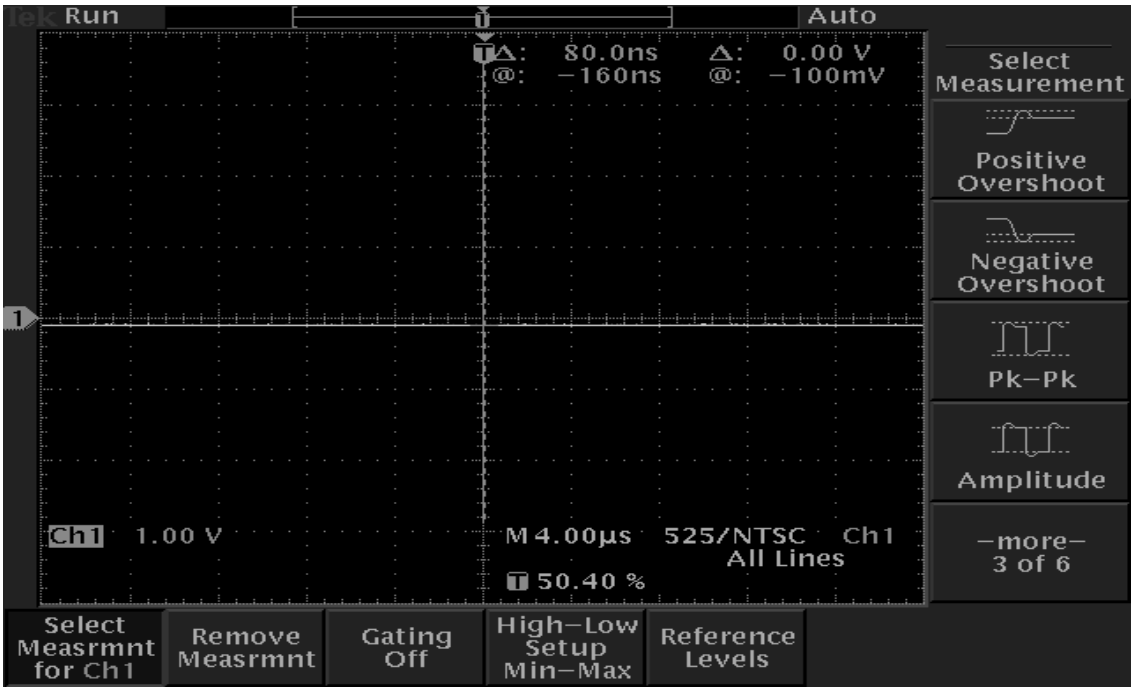


(b)

Figure 4.31. Measured SSB Waveforms. (a) V_A is at -3 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

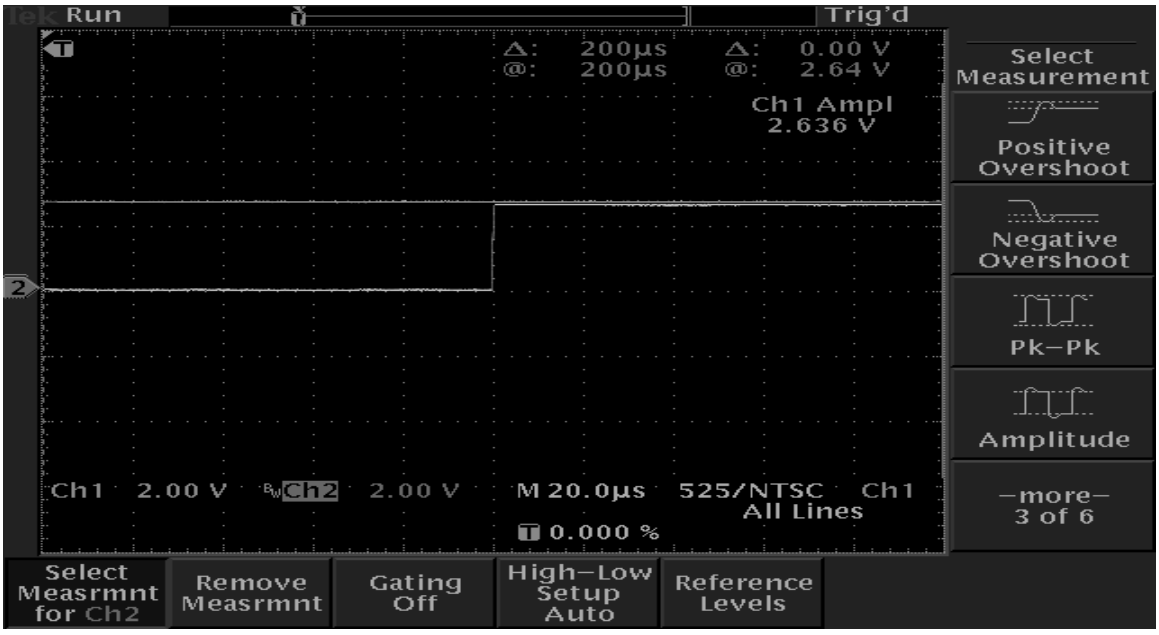


(a)

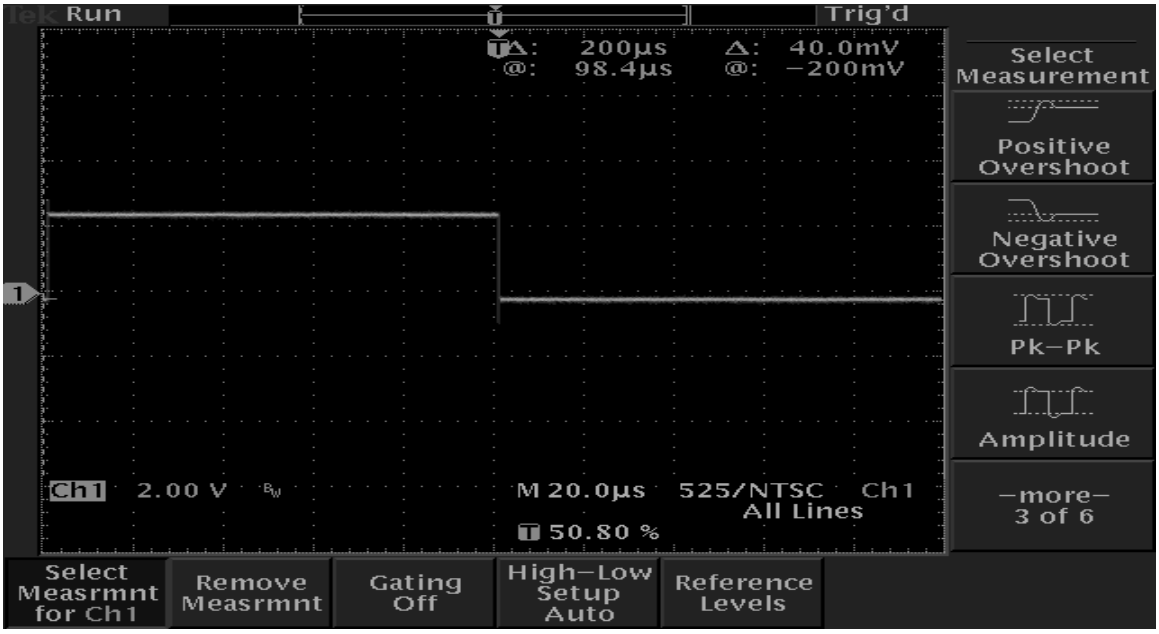


(b)

Figure 4.32. Measured SSB Waveforms. (a) V_A is at 0 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

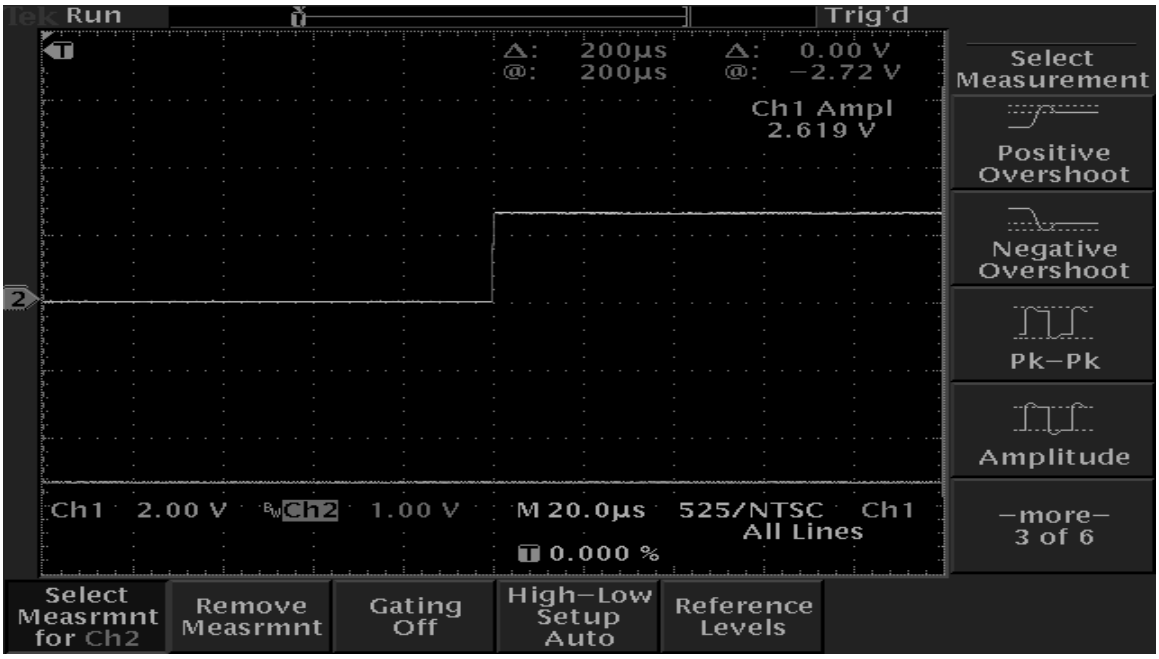


(a)

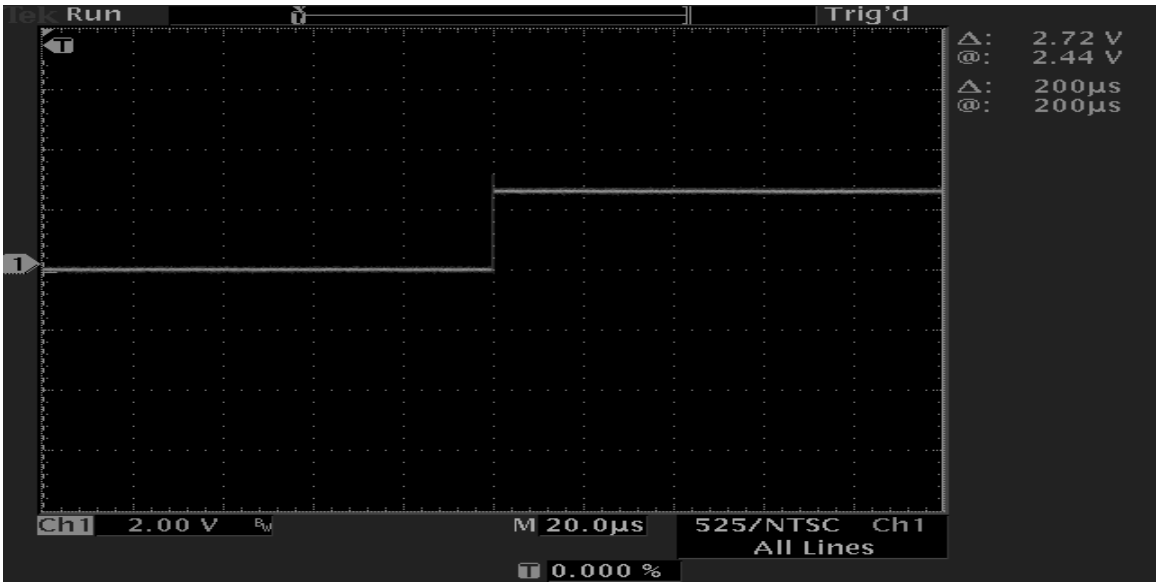


(b)

Figure 4.33. Measured SSB Waveforms. (a) V_A is at 3 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

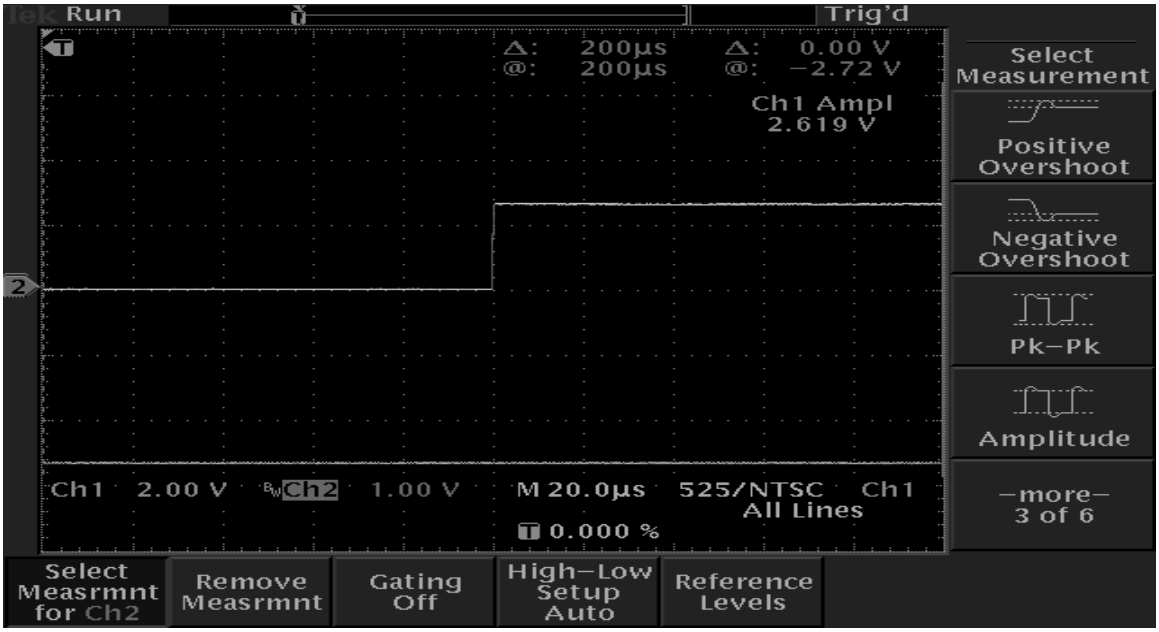


(a)

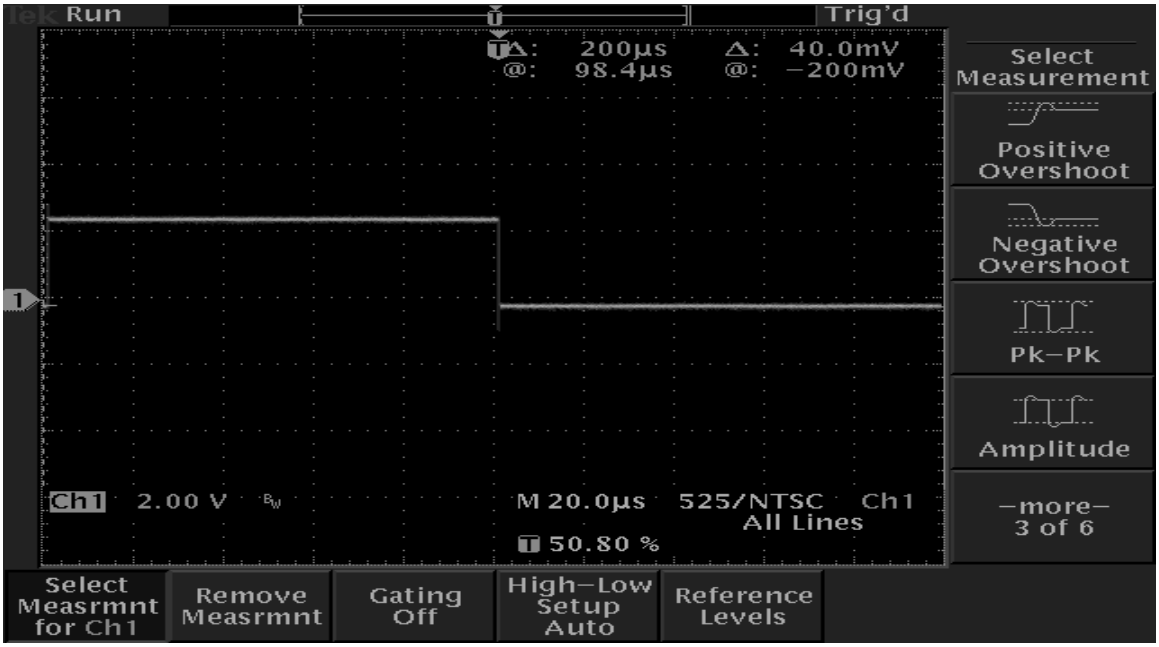


(b)

Figure 4.34. Measured SSB Waveforms. (a) V_B is at -3 V and V_A Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

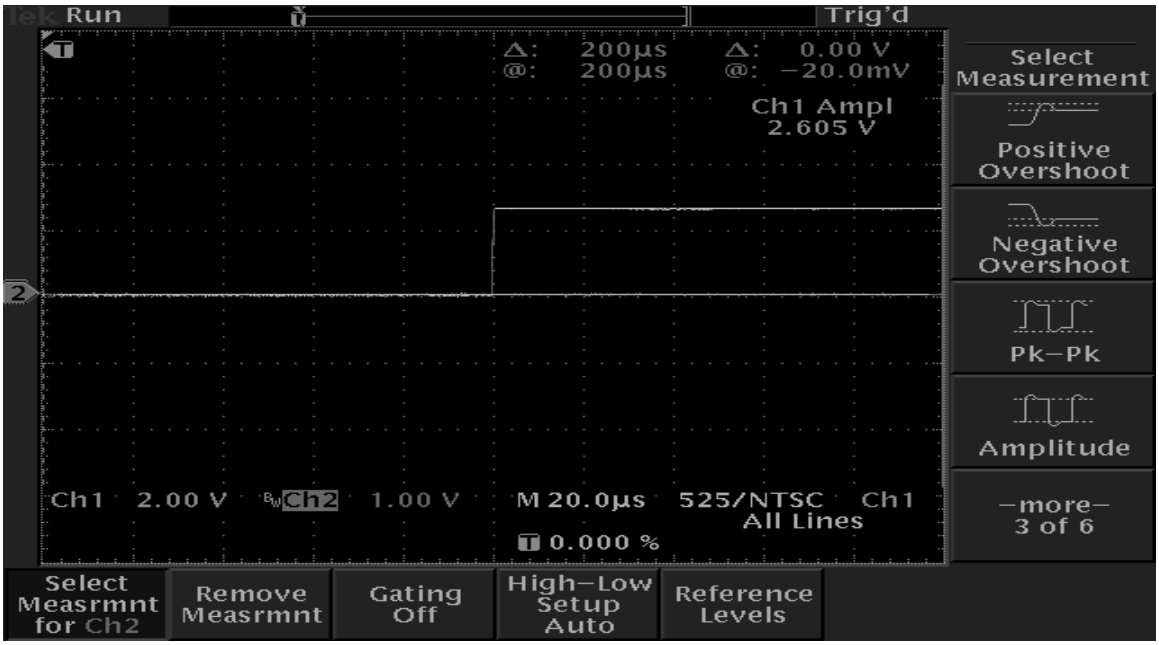


(a)

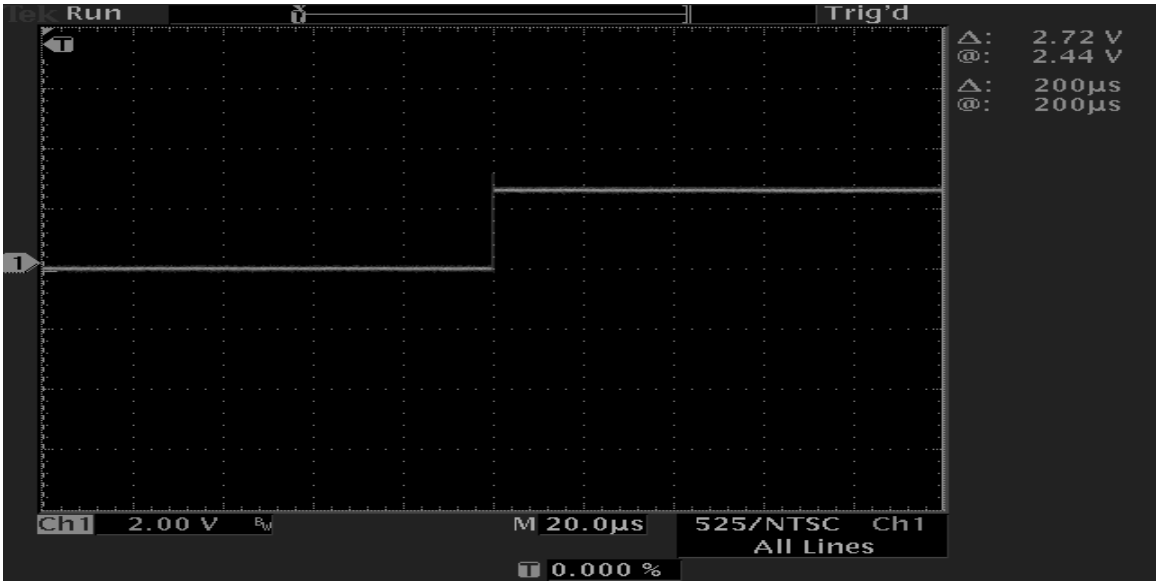


(b)

Figure 4.35. Measured LSB Waveforms. (a) V_A is at -3 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

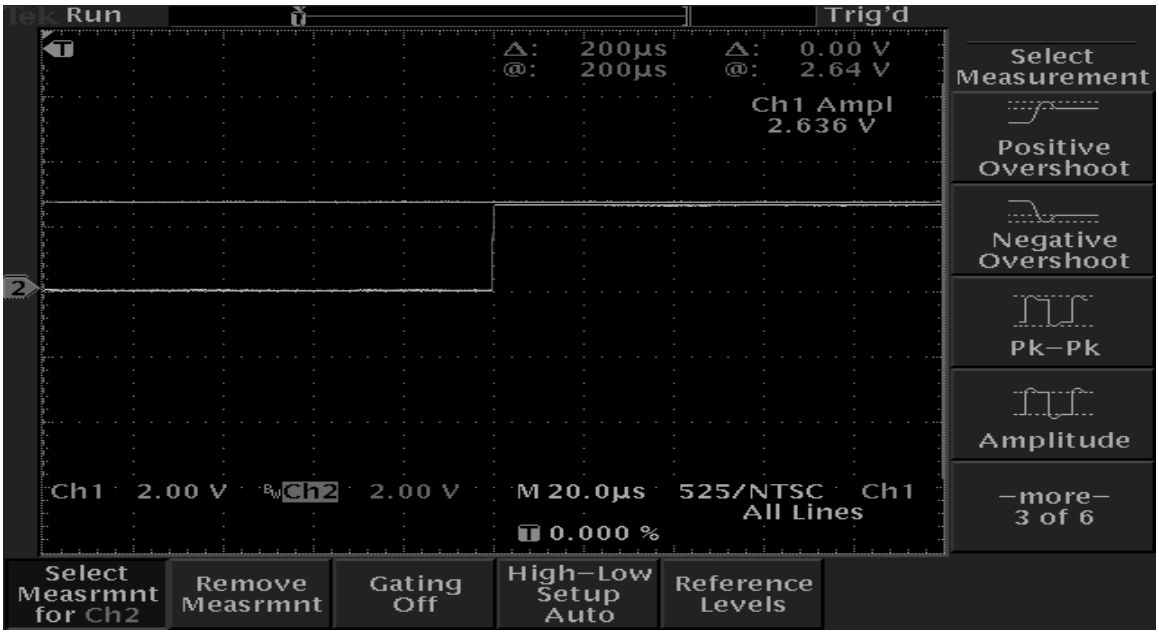


(a)

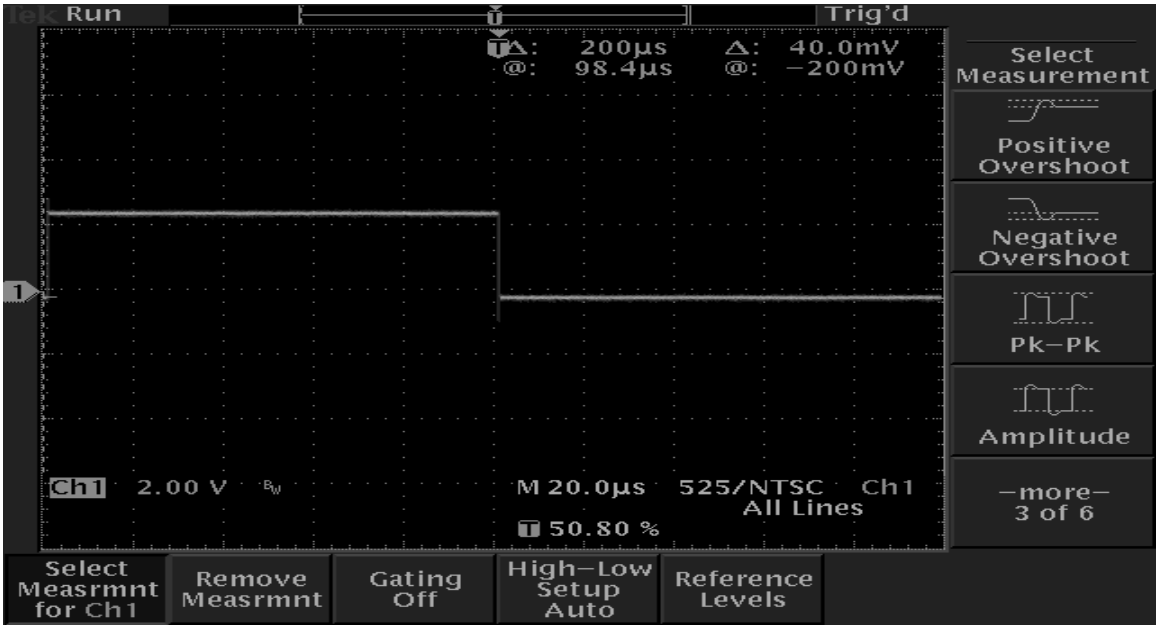


(b)

Figure 4.36. Measured LSB Waveforms. (a) V_A is at 0 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

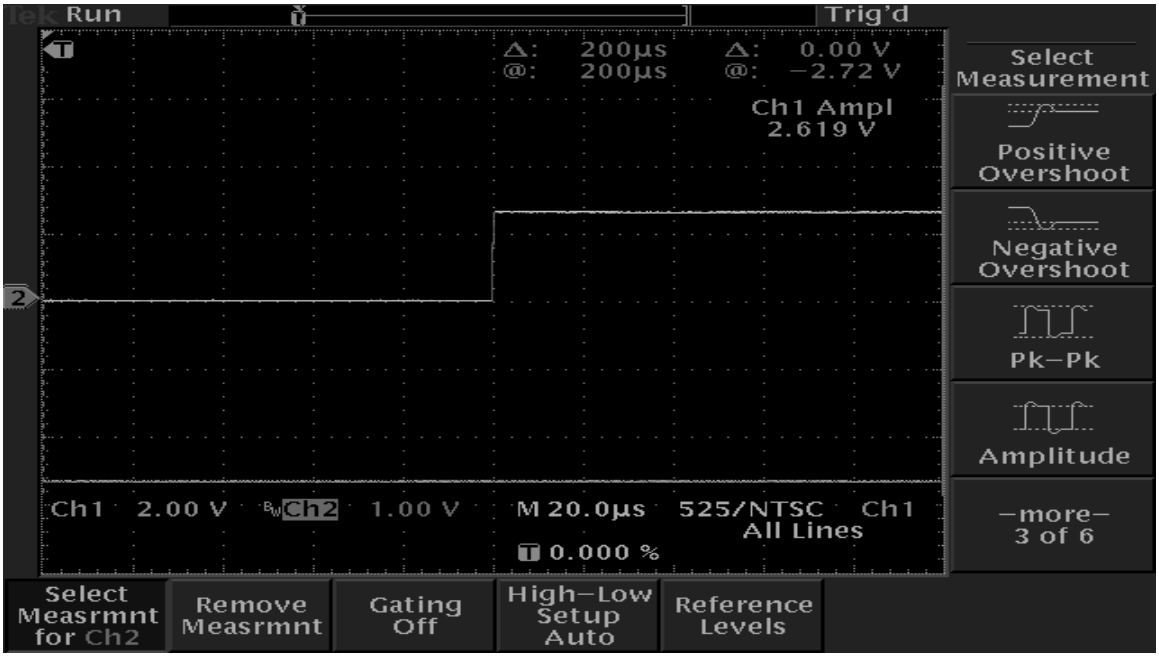


(a)

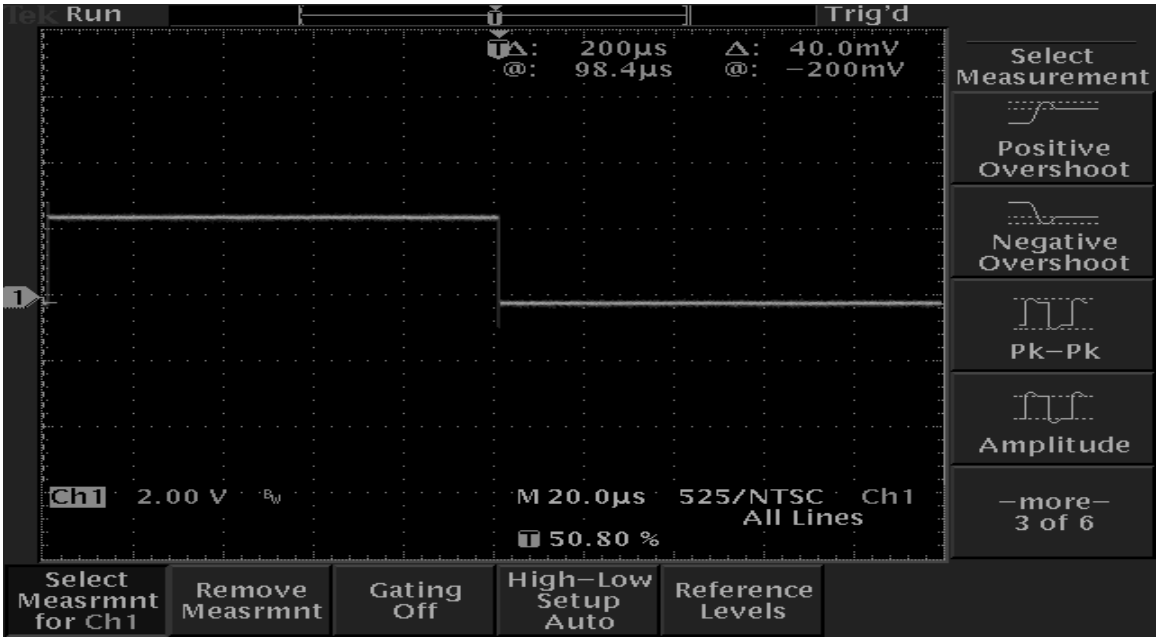


(b)

Figure 4.37. Measured LSB Waveforms. (a) V_A is at 3 V and V_B Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).



(a)



(b)

Figure 4.38. Measured LSB Waveforms. (a) V_B is at -3 V and V_A Varying from 0 V to 3 V and (b) Output Waveform for Input Condition Shown in (a).

Chapter 5. Conclusions and Future Work

5.1 Conclusion

An integrated circuit design is presented for the conversion of ternary logic to binary bits using multiple input floating gate MOSFETs in CMOS. The floating potential diagrams for the various stages of the converter have been used as the building blocks of the conversion circuit. Weighted sum of all inputs at each gate is calculated. The switching transistor turns ON or OFF depending upon the calculated voltage being greater than or less than the switching threshold voltage. The switching threshold was modulated bearing in mind the fact that the floating gate capacitors act like memory devices and tend to store charge on the gate. In this thesis, a simple method is proposed, wherein a bias is applied to the floating gate and the charge is modulated to achieve the desired output. The circuit has been designed for balanced ternary logic (-1 0 +1) using a 250 fF unit capacitor and fabricated in standard 0.5 μm digital n-well CMOS technology. The circuits are simulated in Cadence PSPICE version 15 with MOSIS BSIM level 49 model parameters. L-Edit version 10.2 was used in layout and uses a total of 26 transistors. The converter chip occupies an area of 1434.43 μm^2.

5.2 Future Work

An important aspect of the present design is to modulate the floating gate bias voltages. A circuit which nullifies the floating gate charge controlled by a clock may be devised in order to have adaptive circuits. The charge on the floating gate can be removed by adding a clocked n-MOS transistor to the inverter which discharges the gate voltage every time the input changes.

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Appendix

A. P-SPICE circuit input files

Following is the PSpice input file of the floating gate CMOS inverter shown in fig.C.1.

* Circuit file to obtain the I-V Characteristics of floating gate nMOS transistor.

```
C1 gate1 gate 250.0f
r gate gate1 1e12
M3 drain gate 0 0 NMOS L=2.1u W=4.2u
VDS drain1 0
VGS gate1 0
VIDS drain1 drain
.DC Lin VGS 0 3 .03 Lin VDS 0 3 1
.probe
.end
```

*Circuit file used to obtain the I-V Characteristics of floating gate pMOS transistor

```
r gate gate1 1e12
C1 gate1 gate 250.0f
M3 drain gate 0 0 PMOS L=2.1u W=4.2u
VDS drain1 0
VGS gate1 0
VIDS drain1 drain
.DC Lin VDS 0 -3 -.03 VGS 0 -3 -1
.probe
.end
```

*Circuit file to obtain the voltage transfer characteristics of floating gate CMOS inverter

```
Vin 1 0
Vdd 2 0 3.0v
Vss 4 0 0v
r 1 5 1e20
C4 1 5 250.71918f
M3 3 5 2 2 PMOS L=2.1u W=20.35u
M1 3 5 4 4 NMOS L=2.1u W=4.2u
.probe
.dc Vin 0 3 .1
.END
```

B. P-spice MOSFET model parameters

*Mosfet Model Parameters fro nmos and pmos given by MOSIS

```
.MODEL NMOS NMOS (LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 1.42E-8
+XJ      = 1.5E-7       NCH     = 1.7E17      VTH0    = 0.6377641
+K1      = 0.8706769    K2      = -0.0982359  K3      = 21.6936895
+K3B     = -8.0574052   W0      = 1E-8        NLX     = 1E-9
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 3.0263766    DVT1    = 0.4752173   DVT2    = -0.1322677
+U0      = 460.7911298  UA      = 1E-13       UB      = 1.524291E-18
+UC      = 8.176447E-12 VSAT    = 1.555698E5  A0      = 0.5330678
+AGS     = 0.1130957    B0      = 2.766526E-6 B1      = 5E-6
+KETA    = -1.271567E-3 A1      = 3.170847E-4 A2      = 0.4056523
+RDSW    = 1.488343E3   PRWG    = 0.0188986   PRWB    = 0.0172943
+WR      = 1            WINT    = 2.817629E-7 LINT    = 3.531541E-8
+XL      = 0            XW      = 0           DWG     = -1.61448E-8
+DWB     = 4.485855E-8  VOFF    = -3.147434E-3 NFACTOR = 1.0343323
+CIT     = 0            CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.0196943   ETAB    = -1.388605E-3
+DSUB    = 0.2220415    PCLM    = 2.3266703   PDIBLC1 = -0.2707988
+PDIBLC2 = 2.945029E-3  PDIBLCB = -8.492381E-3 DROUT   = 0.5680404
+PSCBE1  = 5.427038E8   PSCBE2  = 3.680084E-5 PVAG    = 0
+DELTA   = 0.01         RSH     = 81.9        MOBMOD  = 1
+PRT     = 0            UTE     = -1.5        KT1     = -0.11
+KT1L    = 0            KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0            WLN     = 1           WW      = 0
+WWN     = 1            WWL     = -6.554E-20  LL      = 0
+LLN     = 1            LW      = 0           LWN     = 1
+LWL     = -9.461E-20   CAPMOD  = 2           XPART   = 0.4
+CGDO    = 2.07E-10     CGSO    = 2.07E-10    CGBO    = 1E-9
+CJ      = 4.214693E-4  PB      = 0.980151    MJ      = 0.4443288
+CJSW    = 3.272714E-10 PBSW    = 0.1         MJSW    = 0.1148299
+CF      = 0            PVTH0   = -0.0842684  PRDSW   = -402.7051438
+PK2     = -0.0232735   WKETA   = -0.0242589  LKETA   = 2.958034E-3  )
*
.MODEL PMOS PMOS (LEVEL   = 7
+VERSION = 3.1          TNOM    = 27          TOX     = 1.42E-8
+XJ      = 1.5E-7       NCH     = 1.7E17      VTH0    = -1.0231969
+K1      = 0.5212672    K2      = 0.0171704   K3      = 6.1288047
+K3B     = -1.2177527   W0      = 1E-8        NLX     = 1.706664E-8
```

```
+DVT0W   = 0            DVT1W   = 0            DVT2W   = 0
+DVT0    = 3.1928296    DVT1    = 0.6286414    DVT2    = -0.100348
+U0      = 249.4853502  UA      = 3.826857E-9  UB      = 1E-21
+UC      = -5.35409E-11 VSAT    = 1.993208E5   A0      = 0.9677168
+AGS     = 0.1693068    B0      = 1.17117E-6   B1      = 3.67199E-6
+KETA    = -3.399321E-3 A1      = 0            A2      = 0.3
+RDSW    = 3E3          PRWG    = -0.054791    PRWB    = -0.0729412
+WR      = 1            WINT    = 3.78583E-7   LINT    = 2.716131E-8
+XL      = 0            XW      = 0            DWG     = -3.992743E-8
+DWB     = 4.86879E-9   VOFF    = -0.0776484   NFACTOR = 0.745962
+CIT     = 0            CDSC    = 2.4E-4       CDSCD   = 0
+CDSCB   = 0            ETA0    = 6.066371E-4  ETAB    = 2.304032E-5
+DSUB    = 0.0271462    PCLM    = 2.3314756    PDIBLC1 = 0.1139082
+PDIBLC2 = 2.190674E-3  PDIBLCB = -0.1         DROUT   = 0.3246629
+PSCBE1  = 5.144178E9   PSCBE2  = 5.047658E-10 PVAG    = 0.6854127
+DELTA   = 0.01         RSH     = 106.9        MOBMOD  = 1
+PRT     = 0            UTE     = -1.5         KT1     = -0.11
+KT1L    = 0            KT2     = 0.022        UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11     AT      = 3.3E4
+WL      = 0            WLN     = 1            WW      = 0
+WWN     = 1            WWL     = -1.205E-20   LL      = 0
+LLN     = 1            LW      = 0            LWN     = 1
+LWL     = 6.268E-21    CAPMOD  = 2            XPART   = 0.4
+CGDO    = 2.79E-10     CGSO    = 2.79E-10     CGBO    = 1E-9
+CJ      = 7.294625E-4  PB      = 0.9509988    MJ      = 0.4952483
+CJSW    = 2.549068E-10 PBSW    = 0.99         MJSW    = 0.2932858
+CF      = 0            PVTH0   = 5.98016E-3   PRDSW   = 14.8598424
+PK2     = 3.73981E-3   WKETA   = 7.226797E-3  LKETA   = -3.642511E-3  )
*
```

C. Circuit Diagram for the Floating Node

The bias voltage x_i V for various stages (i = 1 to 11) was applied to the floating gate of each stage such that the existing floating gate potential Φ_f is corrected to Φ_c. The circuit diagram for the application of the bias voltage is shown in Figure C1**.** When the circuit is simulated in PSPICE it fails to converge at the floating gate. Hence a large resistance, R, in the range of 1E12 ohms was placed from floating gate node to ground as shown in Figure C.1. The resistor gives the effect of open circuit from floating gate to ground.

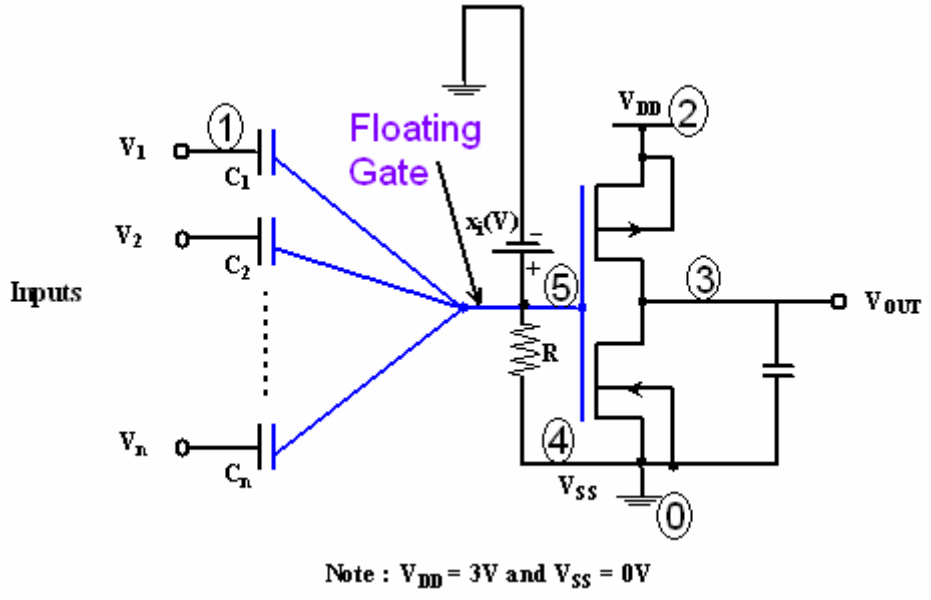

Figure C.1

D. PSpice circuit input file for a floating gate CMOS inverter.

Following is the PSPICE input file of a floating gate CMOS inverter shown in Figure C.1.

```
Va 4 0 pwl(0n -3v  300n -3v 300.1n 0v 600n 0v 600.1n 3v 900n 3v)
Vb 5 0 pwl(0n 3.0v 0.1n -3v 100n -3v 100.1n 0v 200n 0.0V 200.1n 3v 300n 3v 300.1n -
3v 400n -3v 400.1n 0.0v 500n 0.0v 500.1n 3v
+ 600n 3v 600.1n -3v 700n -3v 700.1n 0.0v 800n 0.0v 800.1n 3v)
Vdd 2 0 DC 3v
Vss 6 0 DC 0v
r 1 0 1e20
M8 2 1 3 2 PMOS L=2.1u W=20.35u
C5 2 1 1250.391f
M3 6 1 3 6 NMOS L=2.1u W=4.2u
C2 4 1 750.27742f
C1 5 1 250.71918f
.probe
.tran 0n 900n
.ic v(1)= 1.0V
.END
```

Vita

Sowmya Subramanian was born in Andhra Pradesh, on 6th November 1980, India. She earned her primary and secondary education from St. Ann's High School in Hyderabad, Andhra Pradesh. She then went on to procure her bachelor's degree in Electrical and Electronics Engineering from Jawarharlal Nehru Technological University (JNTU) in spring 2002. After her graduation, she came to United States of America to pursue her master's degree in electrical engineering. She joined the graduate program at Louisiana State University, Baton Rouge, in August 2002. She is a candidate for the degree of Master of Science in Electrical Engineering to be awarded at the commencement of Fall 2005.